User's Manual

ECB-865

Intel 815E Tualatin Pentium III / Celeron Full-size CPU Card

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Part No.2047865000

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5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

- 1 ECB-865 Full-size Celeron / Pentium III single board
- 1 Quick Installation Guide
- 1 CD-ROM contains the followings:
  - User's Manual (this manual in PDF file)
  - Ethernet driver and utilities
  - VGA drivers and utilities
  - Latest BIOS (as of the CD-ROM was made)
- Cable set includes the followings:
  - 1 IDE HDD cable (40-pin, pitch 2.54mm)
  - 1 FDD cable (34-pin, pitch 2.54mm)
  - 1 bracket with one Printer port cable (26-pin, pitch 2.54mm) and one Serial port cable (10-pin, pitch 2.0mm)
  - 1 bracket with two Serial port cable (10-pin, pitch 2.54mm)
  - 1 5-pin to 5-pin keyboard cable for passive backplane connection
  - 1 4-pin ATX power control cable for backplane connection

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

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Document Amendment History

Revision	Date	By	Comment
1st	Feb. 02.	Harris Chen	Initial Release

1. Manual Objectives

This manual describes in detail the Evalue Technology ECB-865 Single Board.

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard IBM Technical References, unless it proved to be necessary to aid in the understanding of this board. The manual is sectioned and includes a User's Guide that will help the non-technical user to get the unit up and running. A Troubleshooting Guide is also included to help when things go wrong.

We strongly recommend that you study this manual carefully before attempting to interface with ECB-865 or change the standard configurations. Whilst all the necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier for guidance.

Please be aware that it is possible to create configurations within the CMOS RAM that make booting impossible. If this should happen, clear the CMOS settings, (see the description of the Jumper Settings for details).

If you have any suggestions or find any errors concerning this manual and want to inform us of these, please contact our Customer Service department with the relevant details.

2. Introduction

2.1 System Overview

The ECB-865 is an all-in-one Full-size Pentium III / Celeron Single Board Computer (SBC) designed with Intel embedded chipset 815E-B which supports the latest Intel FC-PGA/FC-PGA2 Pentium III / Celeron processor (CopperMine and Tualatin) up to 1.1GHz or above and AGP 4X 3D Graphics Accelerator w/ shared display memory of 4MB SDRAM, dual Intel PCI-bus Fast Ethernet controllers, and M-Systems DiskOnChip socket.

Targeting on the mission critical telecommunication or industrial applications, the ECB-865 comes designed with Intel EMD solutions. These include Intel 815E-B AGPset, 82562ET PLC and 82559 10/100Base-Tx Fast Ethernet controller. Unlike regular commercial solutions, Intel EMD solutions provide higher system stability and longer product supply time (Intel EMD products' typical life cycle is 5 years). The long product life cycle guarantee is particularly important for systems that are designed to last for many years. This makes it a perfect solution for not only popular Networking Devices like Firewall, Gateway, Router, and e-Server, but also CTI (Computer Telephony Integration) equipments such as PBX, Digital Logger, etc.

Other onboard features include PC133 FSB, Address/Data buffer to enhance the ISA-bus driving capacity up to 64mA, dual UDMA 100 IDE channels, two 16C550 compatible serial ports (one RS-232, one RS-232/422/485), one multi-mode parallel port, three 168-pin DIMM sockets allowing for up to 1.5GB of SDRAM to be installed, and on-board proprietary PCI interface for optional PCI module expansion. The PCI modules currently available are Adaptec 7892 Ultra 160 SCSI, and Intel 82559 10/100Base-Tx Ethernet modules

2.2 System Specifications

General Functions

- **Bus Interface:** PICMG 2.0 Compliant
- **ISA Driving Capacity:** Built-in Address/Data buffer supports driving capacity up to 64mA
- **CPU:** Supports Intel FCPGA/FCPGA2 Pentium III / Celeron processor up to 1GHz or above (with system bus frequencies of 66/100/133MHz)
- **CPU Socket:** Intel FC Socket 370
- **BIOS:** AMI 4Mb FWH BIOS
- **Chipset:** Intel 815E-B AGPset
- **I/O Chipset:** ITE IT8712F-A
- **Memory:** Onboard three 168-pin DIMM sockets support up to 1.5Gbytes SDRAM
- **Enhanced IDE:** Supports up to four IDE devices. Supports Ultra DMA 33/66/100 mode with data transfer rate up to 100MB/sec. (20 x 2 header x 2 onboard)
- **FDD Interface:** Supports up to two floppy disk drives, 5.25" (360KB and 1.2MB) and/or 3.5" (720KB, 1.44MB, and 2.88MB)
- **Parallel Port:** One bi-directional parallel port. Supports SPP, ECP, and EPP modes
- **Serial Port:** One RS-232 serial ports and one RS-232/422/485 serial port. Ports can be configured as COM1, COM2, COM3, COM4, or disabled individually. (16C550 equivalent)
- **IR Interface:** Supports one IrDA Tx/Rx header
- **KB/Mouse Connector:** One 6-pin mini-DIN connector supports PS/2 keyboard and mouse
- **USB Connectors:** Two 5 x 2 header onboard support up to four USB ports
- **Smart Card Reader Connector:** One 7 x 2 header onboard support a Smart Card Reader port
- **Watchdog Timer:** Can generate a system reset, or NMI. Jumper selectable time-out interval (0.5, 1, 2, 4, 8, 16, 32, 64 sec.)
- **DMA:** 7 DMA channels (8237 equivalent)

- **Interrupt:** 15 interrupt levels (8259 equivalent)
- **Hardware Status Monitoring:** Monitoring system temperature, voltage, and cooling fan status. Auto throttling control when CPU overheats
- **Power Management:** Supports ATX power supply. Supports PC98, LAN wake up and modem ring-in functions. I/O peripheral devices support power saving and doze/standby/suspend modes. APM 1.2 compliant

VGA Interface

- **Chipset:** Intel 815E-B 3D Graphics Accelerator
- **Display Memory:** Up to 4MB shared display memory
- **Interface:** AGP 4X, Accelerator Graphics Ports 1.0 compliant
- **Resolution:** 1280 x 1024 @ 24bpp

Ultra 160 SCSI Interface (Optional)

- **Chipset:** Adaptec 7892
- **SCSI Interface:** Supports 32-bit PCI interface and Ultra 160 SCSI or legacy single-ended devices; data transfer rates up to 160MB/sec

Ethernet Interface

- **Chipset:** Intel 82801BA ICH2 built-in and 82559 PCI-bus Ethernet controller onboard support dual Ethernet function
- **Ethernet Interface:** PCI 100/10 Mbps, IEEE 802.3U compatible, dual RJ-45 interfaces
- **Remote Boot-ROM:** For diskless system

SSD Interface

One 32-pin DIP socket supports M-Systems DiskOnChip 2000 series, memory capacity from 8MB to 576MB

Expansion Interface

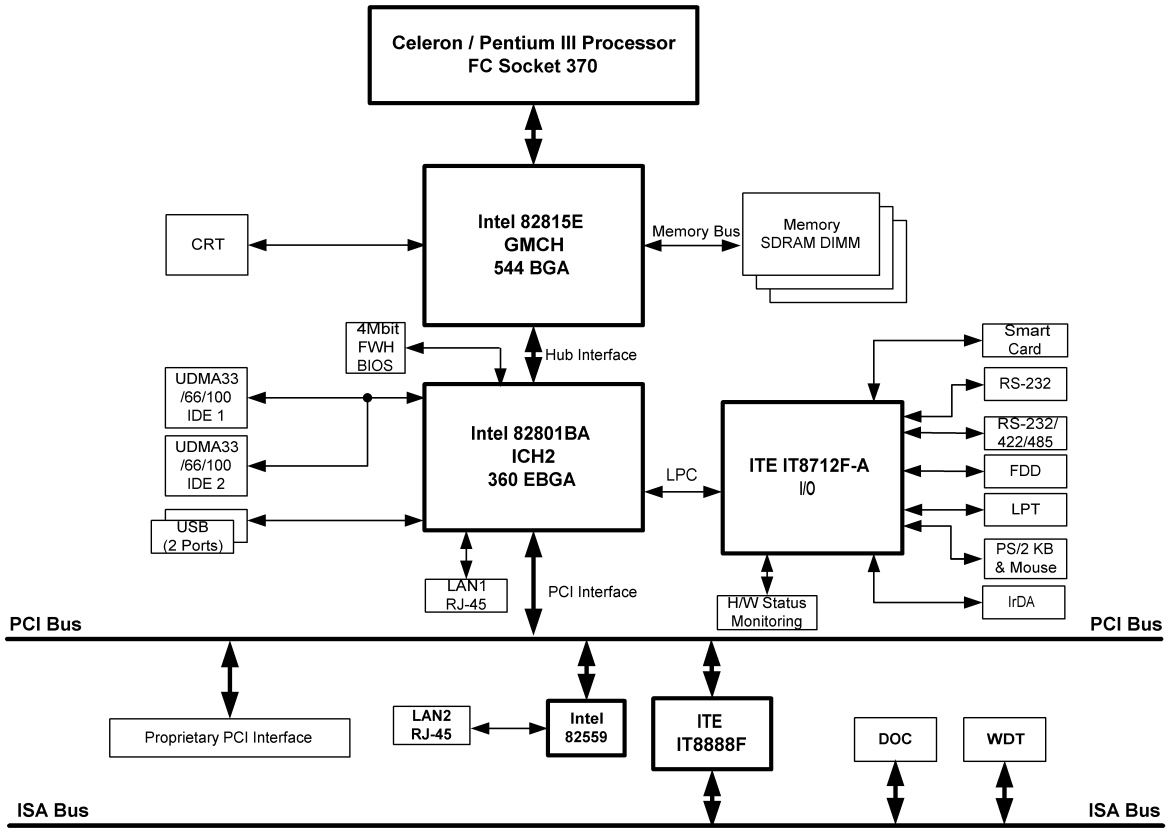
One 80-pin proprietary PCI interface for PCI device expansion

Mechanical and Environmental

- **Power Supply Voltage:** +5V (4.75V to 5.25V), +12V (11.4V to 12.6V), and -12V (-11.4V to -12.6V)
- **Typical Power Requirement:** +5V @ 6.5A, +12V @ 140mA, -12V @ 30mA w/ Intel Celeron 466MHz CPU and 128MB SDRAM
- **Operating Temperature:** 32 to 140 °F (0 to 60 °C)
- **Board Size:** 13.3"(L) x 4.8"(W) (338mm x 122mm)
- **Weight:** 0.5 Kg

2.3 Architecture Overview

The following block diagram shows the architecture and main components of ECB-865. Two major chipsets on board are the 82815E Graph Memory Control Hub and 82801BA ICH2. These two devices provide interface to Socket370 processor, supports CRT display, SDRAM with ECC, PCI bus interface, ACPI compliant power management , USB port, SMBus communication, and Ultra DMA/33/66/100 IDE Bus Master. The onboard super I/O chip, IT8712F-A, supports PS/2 Keyboard/Mouse, two 16C550 UARTs, FDC, Parallel and Infrared interface. In addition, the onboard Intel 82559 10/100BASE-TX Ethernet controller delivers high speed data transfers over the PCI bus.



The following sections provide detail information about the functions provided onboard.

2.3.1 82815 GMCH and 82801BA

The Intel® 815 chipset for use with the universal socket 370 is a high-flexibility chipset designed to extend from the basic graphics/multimedia PC platform up to the mainstream performance desktop platform. The chipset consists of the Intel_ 82815 Graphics and Memory Controller Hub (GMCH) and an I/O Controller Hub (ICH or ICH2) for the I/O subsystem. The GMCH integrates a system memory SDRAM controller that supports a 64-bit 100/133 MHz SDRAM array.

The Intel 82815 GMCH integrates a Display Cache SDRAM controller that supports a 32-bit 133 MHz SDRAM array for enhanced integrated 2D and 3D graphics performance. Multiplexed with the display cache interface is an AGP controller interface to enable graphics configuration and upgrade flexibility with the Intel 815 chipset for use with the universal socket 370. The AGP interface and the internal graphics device are mutually exclusive. When the AGP port is populated with an AGP graphics card, the integrated graphics is disabled; thus, the display cache interface is not needed.

The Intel 815 chipset for use with the universal socket 370 supports the following processors:

- Intel® Pentium® III processor based on 0.18 micron technology (CPUID = 068xh). These processors support the AGTL+ bus interface
- Intel® Celeron™ processor based on 0.18 micron technology (CPUID = 068xh). This applies to Celeron 533A MHz and ≥ 566 MHz processors. These processors support the AGTL+ bus interface.
- Future 0.13 micron socket 370 processors. These processors support the AGTL bus interface.

The 82815 GMCH along with the 82801BA ICH2 provide the basic functionality and buses of the system:

- Interface to SDRAM, 64-bit data bus. Up to 3 double sided DIMMs at 100 MHz system memory bus. Up to 2 double sided or 3 single sided DIMMs at 133 MHz system memory bus.
- PCI Rev 2.2 compliant with support for 33 MHz PCI operations, Supports up to 6 Req/Gnt pairs
- System Management Bus (SMBus) compatible with most I2C devices
- Integrated IDE controller support Ultra ATA/100/66/33 with two 40-pin connectors
- 2 USB ports integrated in ICH2.
- Integrated LAN controller
- AC.97 2.1 compliant link for audio and telephony codecs up to 6 channels
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support

.

2.3.2 DRAM Interface

The GMCH integrates a system memory controller that supports a 64-bit 100/133 MHz SDRAM array. The only DRAM type supported is industry standard Synchronous DRAM (SDRAM). The SDRAM controller interface is fully configurable through a set of control registers. The DRAM controller supports the following features:

- *DRAM type:* Support for x8 and x16 SDRAM device width, Unbuffered, and Non-ECC SDRAM only
- *Memory Size:* 32 MB to 512 MB using 16Mb/64Mb/128Mb/256Mb technology
- *Addressing Type:* Asymmetrical addressing only
- *DRAM Speeds:* 100/133 MHz for synchronous memory (SDRAM).
- *Memory Modules supported:* Up to 3 double-sided DIMMs at 100 MHz system memory bus; Up to 2 double sided or 3 single-sided DIMMs at 133 MHz system memory bus.
- Suspend to RAM support

2.3.3 Multiplexed AGP and Display Cache Interface

The Intel 82815 GMCH multiplexes an AGP interface with a display cache interface for internal 3D graphics performance improvement. The display cache is used only in the internal graphics.
When an AGP card is installed in the system, the GMCH internal graphics will be disabled and the AGP controller will be enabled.

2.3.3.1 AGP Interface

A single AGP connector is supported by the GMCH AGP interface. The AGP buffers operate in one of two selectable modes in order to support the AGP Universal Connector:

- 3.3 V drive, not 5 Volt safe: This mode is compliant to the AGP 1.0 and 2.0 specifications
- 1.5 V drive, not 3.3 Volt safe: This mode is compliant with the AGP 2.0 specification.

The following table shows the AGP Data Rate and the Signaling Levels supported by the GMCH.

Data Rate	Signaling Level	
	1.5 V	3.3 V
1x AGP	Yes	Yes
2x AGP	Yes	Yes
4x AGP	Yes	No

2.3.4 PCI Interface

The ICH2 PCI interface provides a 33 MHz, Rev. 2.2 compliant implementation. All PCI signals are 5V tolerant, except PME#. The ICH2 integrates a PCI arbiter that supports up to six external PCI bus masters in addition to the internal ICH2 requests.

2.3.5 IDE Interface (Bus Master Capability and Synchronous DMA Mode)

The fast IDE interface supports up to four IDE devices providing an interface for IDE hard disks and CD ROMs. Each IDE device can have independent timings. The IDE interface supports PIO IDE transfers up to 14 Mbytes/sec and Bus Master IDE transfers up 100 Mbytes/sec. It does not consume any ISA DMA resources. The IDE interface integrates 16x32-bit buffers for optimal transfers.

The ICH2's IDE system contains two independent IDE signal channels. They can be electrically isolated independently. They can be configured to the standard primary and secondary channels (four devices). There are integrated series resistors on the data and control lines.

Access to these controllers is provided by two standard IDC 40-pin connectors.

2.3.6 USB

The USB controller provides enhanced support for the Universal Host Controller Interface (UHCI). This includes support that allows legacy software to use a USB-based keyboard and mouse. The ICH2 is USB Revision 1.1 compliant. The ICH2 contains two USB Host Controllers. Each Host Controller includes a root hub with two separate USB ports each, for a total of 4 USB ports. The signals are provided by a 5 x 2 header or an optional USB bracket adapter.

2.3.7 Ethernet

2.3.7.1 ICH2 LAN Controller

The ICH2's integrated LAN Controller includes a 32-bit PCI controller that provides enhanced scatter-gather bus mastering capabilities and enables the LAN Controller to perform high speed data transfers over the PCI bus. Its bus master capabilities enable the component to process high level commands and perform multiple operations; this lowers processor utilization by off-loading communication tasks from the processor. Two large transmit and receive FIFOs of 3 KB each help prevent data under runs and overruns while waiting for bus accesses. This enables the integrated LAN Controller to transmit data with minimum interframe spacing (IFS).

The LAN Controller can operate in either full duplex or half duplex mode. In full duplex mode the LAN Controller adheres with the IEEE 802.3x Flow Control specification. Half duplex performance is enhanced by a proprietary collision reduction mechanism.

2.3.7.2 Intel 82559

The Ethernet interface is based on an Intel 82559 Ethernet controller that supports both 10BASE-T and 100BASE-TX. The 82559 consists of both the Media Access Controller (MAC) and the physical layer (PHY) interface combined into a single component solution.

The 32-bit PCI controller provides enhanced scatter-gather bus mastering capabilities and enables the 82559 to perform high speed data transfers over the PCI bus. Its bus master capabilities enable the component to process high level commands and perform multiple operations, which lowers CPU utilization by off-loading communication tasks from the CPU. Two large transmit and receive FIFOs of 3 Kbyte each help prevent data under runs and overruns while waiting for bus accesses. This enables the 82559 to transmit data with minimum interframe spacing (IFS).

2.3.8 ITE IT8712F-A

The Winbond W83977TF-AW Super I/O chip provides most input / output interfaces of the system as the following:

- COM 1/2. RS-232/RS-422/RS-485 driver are used whereby RS-232, RS-422 and RS-485 are provided. Mode can be selected by setting hardware jumper. Drivers use charge pumps whereby only +5V is required
- LPT. Support for SPP, EPP and ECP modes
- Floppy interface
- Keyboard interface
- PS/2 Mouse interface
- IrDA interface for infrared communication. This interface shares the controller of COM2
- Provision of buffered ISA databus for BIOS (denoted *XDBus)*
- NVRam with battery backup for BIOS configuration and real time clock

2.3.9 M-Systems DiskOnChip

M-Systems' DiskOnChip 2000 is a high performance single-chip flash disk in a standard 32-pin DIP package. This unique data storage solution offers cost effective data storage beyond that of traditional hard disks. Perfect for applications with limited space and varying capacity requirements. The DiskOnChip 2000 is simply inserted into a 32-pin DIP socket on your platform board and you have a bootable flash disk.

3. Hardware Configuration

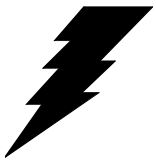
This chapter explains you the instructions of how to set up your system. The additional information shows you how to install M-Systems' DiskOnChip and program the Watchdog Timer.

3.1 Installation Procedure

1. Turn off the power supply.
2. Insert the DIMM module (be careful with the orientation).
3. Insert all external cables for hard disk, floppy, keyboard, mouse, USB etc. except for flat panel. A CRT monitor must be connected in order to change CMOS settings to support flat panel.
4. Connect power supply to the board via the PWR1.
5. Turn on the power.
6. Enter the BIOS setup by pressing the delete key during boot up. Use the "Auto Configuration with Optimal Settings" feature. The ***Peripheral Setup*** and the ***Standard CMOS Setup*** Window must be entered and configured correctly to match the particular system configuration.
7. If TFT panel display is to be utilised, make sure the panel voltage is correctly set before connecting the display cable and turning on the power.

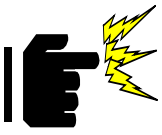
3.2 Safety Precautions

3.2.1 Warning!



Always completely disconnect the power cord from your chassis or power cable from your board whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.

3.2.2 Caution!



Always ground yourself to remove any static charge before touching the board. Modern electronic devices are very sensitive to static electric charges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components in a static-dissipative surface or static-shielded bag when they are not in the chassis.

3.3 Socket 370 Processor

3.3.1 Installing Celeron / Pentium III (Coppermine/Tualatin) CPU

- Lift the handling lever of CPU socket outwards and upwards to the other end.
- Align the processor pins with pin holes on the socket. Make sure that the notched corner or dot mark (pin 1) of the CPU corresponds to the socket's bevel end. Then press the CPU gently until it fits into place. If this operation is not easy or smooth, don't do it forcibly. You need to check and rebuild the CPU pin uniformly.
- Push down the lever to lock processor chip into the socket.
- Follow the installation guide of cooling fan or heat sink to mount it on CPU surface and lock it on the socket 370.
- Be sure to follow particular CPU speed and voltage type to adjust the jumper settings properly.

3.3.2 Removing CPU

- Unlock the cooling fan first.
- Lift the lever of CPU socket outwards and upwards to the other end.
- Carefully lift up the existing CPU to remove it from the socket.
- Follow the steps of installing a CPU to change to another one or place handling bar to close the opened socket.

3.4 Main Memory

ECB-865 provides 3 DIMM sockets (168-pin Dual In-line Memory Module) to support 3.3V SDRAM. The maximum memory size is 1.5GB (registered type of SDRAM). If 100MHz FSB CPU is adopt, you have to use PC-100 SDRAM. For system compatibility and stability, please do not use memory module without brand.

Both single and double-side DIMM module with ECC feature can be used on ECB-865. And, it is not necessary to install the DIMM module in order. You can install different size of SDRAM module on DIMM1, DIMM2, DIMM3, DIMM4 or all.

Watch out the contact and lock integrity of memory module with socket, it will influence the system's reliability. Follow the normal procedure to install your SDRAM module into the DIMM socket. Before locking the DIMM module, make sure that the memory module has been completely inserted into the DIMM socket.

Note:

Please do not change any SDRAM parameter in BIOS setup to increase your system's performance without acquiring technical information in advance.

3.5 M-Systems' DiskOnChip Flash Disk

ECB-865 reserves a 32-pin DIP socket to support M-Systems' DiskOnChip flash disk up to 288 MB. The DiskOnChip is based on pure ISA bus and without PnP (Plug and Play) function. Before the installation, make sure that the DiskOnChip I/O address jumper is set properly to prevent the I/O resource conflict.

3.5.1 Installing DOC

Align the DOC with the pinholes on the socket. Make sure that the notched corner or dot mark (pin 1) of DOC corresponds to notched corner of the socket. Then press the DOC gently until it fits into place. If installation procedure is correct, the flash disk can be viewed as a normal hard disk to access read/write data now.

Note:

Please make sure that your DOC is properly inserted. Place the DOC in wrong direction will damage the flash device.

If you system would like to boot from the flash disk, it is recommended to refer to the application note provided by M-Systems first. You can easily obtain the application note from M-Systems' DiskOnChip user's manual or from their web site as below.

http://www.m-sys.com

3.6 Expansion Interface

The ECB-865 reserves an 80-pin proprietary PCI interface, J22, for PCI device such as LAN, Audio, SCSI, Video Capture expansion in the future. This installation of expansion module is very simple and easy. Without any special tool, all you need to do is just make the board-to-board connection and lock up the screw. For more information about the expansion module, please refer to the instruction manual attached with each module.

3.7 Installing the Single Board Computer

To install your ECB-865 into chassis or proprietary environment, the following steps have to be followed.

- Make sure all jumpers are properly set.
- Install and configure CPU and memory module correctly.
- Place the ECB-865 into the dedicated position in your system.
- Attach cables to peripherals.

Note:

Please ensure that your SBC is properly installed and fixed by mechanism. Otherwise, the system might be unstable or do not work due to bad contact of golden finger and slot.

3.7.1 815E integrated Graphics Controller

The on-board graphics controller integrated in 815E(GMCH) chipset that integrates high performance memory technology for the graphics frame buffer. 32 –bit data interface,133 Mhz SDRAM interface only.Flexible AGP in-line Memory Module (AIMM) implementation. support for two1M X16,or one 2M X32,4MB maximum addressable, thus increasing the available memory bandwidth for the graphics subsystem to support high color/high resolution application. The ECB-865 is designed to support high performance graphics and video acceleration for all supported display resolutions, display types, and color modes on CRT monitor.

The 815E supports the modes which appear in the table below.

Resolution	Bits Per Pixel (frequency in Hz)		
	8-bit Indexed	16-bit	24-bit
320x200	70	70	70
320x240	70	70	70
352x480	70	70	70
352x576	70	70	70
400x300	70	70	70
512x384	70	70	70
640x400	70	70	70
640x480	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
720x480	75,85	75,85	75,85
720x576	60,75,85	60,75,85	60,75,85
800x600	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
1024x768	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
1152x864	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
1280x720	60,75,85	60,75,85	60,75,85
1280x960	60,75,85	60,75,85	60,75,85
1280x1024	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
1600x900	60,75,85	60,75,85	
1600x1200	60,70,72,75		

3.7.2 Intel 82559(or REALTEK RTL8139C) & 82801BA(ICH2) + 82562ET (PHY) Network Controller

The 82559 (or RTL8139C) and ICH2+PHY is fully integrated 10BASE-T/100BASE-TX LAN solution. The 32-bit PCI controller provides enhanced scatter-gather bus mastering capabilities and enables the 8139C to perform high-speed data transfers over the PCI bus. Its bus master capabilities enable the component to process high level commands and perform multiple operations, which lower CPU utilization by off-loading communication tasks from the CPU.

The ECB-865 equips two LED indicators on the RJ-45 connector to indicate the LAN interface status. These messages will provide you a guide for troubleshooting.

Green LED LAN Activity LED that indicates the data transfer activity.

Blinking: indicates transmission/receiving activity

On: indicates no activity but link is valid

Off: link is invalid

Yellow LED LAN Link Integrity LED that indicates link speed

On: link speed at 100Mbps

Off: link speed at 10Mbps

3.7.3 Drivers Support

ECB-865 provides on CD-Title to support on-board VGA and Ethernet device drivers in various operating systems. Before installing the device drivers, please see the reference files in each sub-directory. You cannot install drivers from CD-Title directly.

- **815E CHIPSET INTEGRATED GRAPHY: Support NT4.0, Windows9x, Win2000, … environment**
- **INTEL 815E & ICH2 CHIPSET DRIVER: Support NT4.0, Windows9x, Win2000, … environment**
- **Intel 82559 (or REALTEK 8139C): Support Dos, Windows3.1, Windows9x, NT3.5, NT4.0, Novell, OS/2 …**

3.8 Watchdog Timer Programming

When the **W**atch-**D**og **T**imer (**WDT**) function is enabled, a system reset will be generated unless an application triggers the timer periodically within time-out period. This allows the system to restart in an orderly way in case of any abnormal condition is found.

An optional two-port WDT is provided on ECB-865. This WDT comes with 8 possible ranges of time intervals from 500ms to 64sec., which can be adjusted by setting jumper positions. It could be enabled and programmed by reading I/O port 0533H or 0543H to issue trigger continuously, and disabled by reading I/O port 0033H or 0343H. A tolerance of 30% timer limit must be considered. For instance, if the time-out interval is set to 1 second, the WDT trigger command must be issued within 700ms at least.

The below example gives you a reference algorithm for WDT programming via I/O port 0533H and 0033H in your application programs:

Enable WDT

```
MOV     DX, 0533H
IN      AL, DX
```

Re-trigger WDT

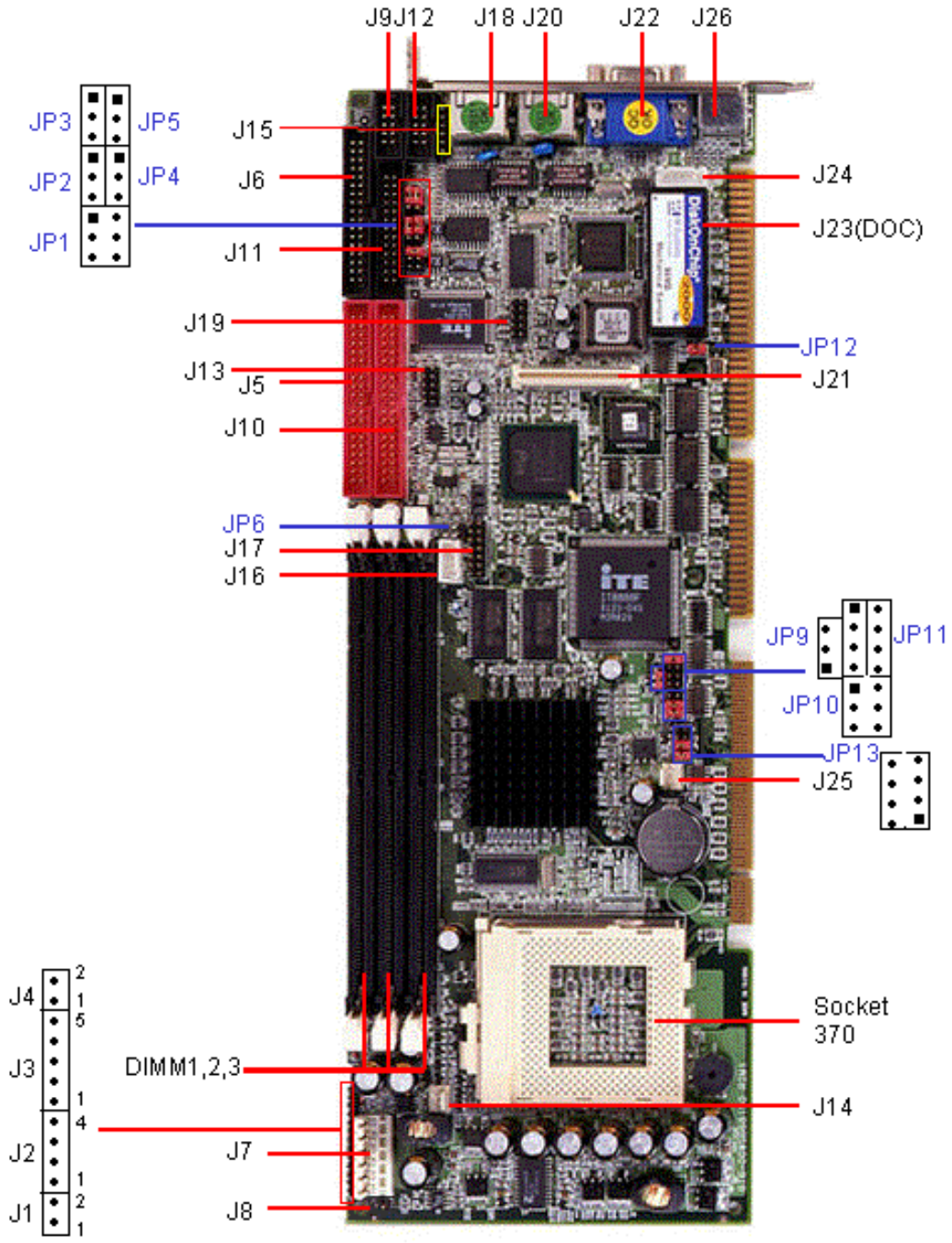
```
MOV     DX, 0533H
IN      AL, DX
```

Disable WDT

```
MOV     DX, 0033H
IN      AL, DX
```

3.9 Jumper & Connector

3.9.1 Jumper & Connector Layout



3.9.2 Jumper & Connector List

Connectors on the board are linked to external devices such as hard disk drives, keyboard, mouse, or floppy drives. In addition, the board has a number of jumpers that allow you to configure your system to suit your application.

The following tables list the function of each of the board's jumpers and connectors.

Jumpers		
Label	**Function**	**Note**
JP1	Serial port RS-232/422/485 select	3 x 2 header, pitch 2.54mm
JP2~JP5	Serial port RS-232/422/485 select	3 x 1 header, pitch 2.54mm
JP6	Watchdog timer select	2 x 1 header, pitch 2.54mm
JP9	Clear CMOS	3 x 1 header, pitch 2.54mm
JP10	Watchdog timer select	3 x 2 header, pitch 2.54mm
JP11	M-Systems DiskOnChip memory address select	4 x 2 header, pitch 2.54mm
JP12	Watchdog timer select	2 x 1 header, pitch 2.54mm
JP13	Proprietary PCI Bus Master Selection	4 x 2 header, pitch 2.54mm

Connectors		
Label	**Function**	**Note**
J1	System reset connector	2 x 1 header, pitch 2.54mm
J2	External speaker connector	4 x 1 header, pitch 2.54mm
J3	Keyboard lock and power indicator connector	4 x 1 header, pitch 2.54mm
J4	Primary IDE / Secondary IDE active indicator connector	2 x 1 header, pitch 2.54mm
J5	Primary IDE connector	20 x 2 header, pitch 2.54mm
J6	Floppy connector	17 x 2 header, pitch 2.54mm
J7	AT power button connector	
J8	ATX power button interface to backplane	2 x 1 header, pitch 2.54mm
J9	Serial port 1 connector	5 x 2 header, pitch 2.54mm
J10	Secondary IDE connector	20 x 2 header, pitch 2.54mm
J11	Parallel port connector	5 x 2 header, pitch 2.54mm
J12	Serial port 2 connector	5 x 2 header, pitch 2.54mm
J13	USB connector	5 x 2 header, pitch 2.54mm
J14	CPU fan connector	3 x 1 wafer, pitch 2.54mm
J15	Fast and standard IrDA (Infrared) connector	6 x 1 header, pitch 2.54mm
J16	ATX power control connector	4 x 1 wafer, pitch 2.54mm
J17	Smart card reader connector	7 x 2 header, pitch 2.54mm
J18	10/100Base-Tx Ethernet connector 1	RJ-45 6-pin mini DIN
J19	USB connector	5 x 2 header, pitch 2.54mm
J20	10/100Base-Tx Ethernet connector 2	RJ-45
J21	Proprietary PCI connector	
J22	CRT connector	DB-15 female connector
J23	M-Systems DiskOnChip socket	16 x 2 DIP socket
J24	Internal keyboard connector	5 x 1 wafer, pitch 2.54mm
J25	System fan connector	3 x 1 wafer, pitch 2.54mm
J26	PS/2 keyboard connector	6-pin mini DIN

3.10 Setting Jumpers

You can configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch.

It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To "close" a jumper you connect the pins with the clip. To "open" a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case, you would connect either two pins.

The jumper settings are schematically depicted in this manual as follows:

A pair of needle-nose pliers may be helpful when working with jumpers.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

3.10.1 Clear CMOS (JP9)

You can use JP9 to clear the CMOS data if necessary. To reset the CMOS data, short JP1 for just a few seconds, and then remove the jumper back to open.

Clear CMOS (JP1)		
	Protect*	Clear CMOS
JP1		

* default

3.10.2 Watchdog Timer

3.10.2.1 Enable / Disable Onboard Watchdog Timer (JP12)

You can use JP12 to enable / disable the onboard Watchdog timer function if necessary. To disable the onboard Watchdog timer function, short JP12, to enable the function of Watchdog timer, set JP12 to open.

Enable / Disable Onboard Watchdog Timer (JP12)		
	Enable	Disable*
JP12		

* default

3.10.2.2 Watchdog Timer Programming I/O Address Select (JP6)

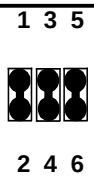
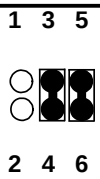
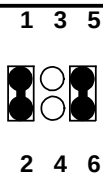
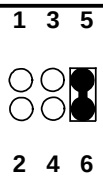
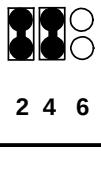
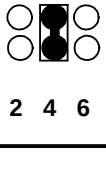
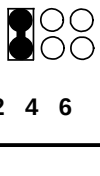
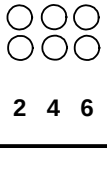
You can set JP6 to select the Watchdog timer programming I/O address. The choice is 0553H / 0033H and 0543H / 0343H.

Watchdog Timer Programming I/O Address Select (JP6)		
	0553H / 0033H*	0543H / 0343H
JP6		

* default

3.10.2.3 Watchdog Timer Time-Out Interval Select (JP10)

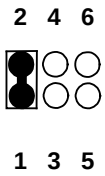
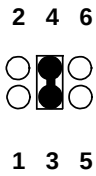
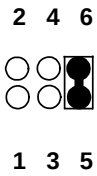
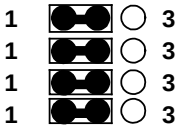
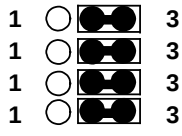
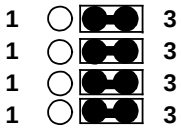
You can set JP10 to select the Watchdog timer time-out interval to be 0.5, 1, 2, 4, 8, 16, 32, or 64 Sec.

Watchdog Timer Tim-Out Interval Select (JP10)				
	0.5 Sec.	1 Sec. *	2 Sec.	4 Sec.
JP10				
	8 Sec.	16 Sec.	32 Sec.	64 Sec.
				

* default

3.10.3 COM2 RS-232/422/485 Select (JP1, JP2~JP5)

The ECB-865 COM2 serial port can be selected as RS-232, RS-422, or RS-485 by setting JP1 & JP2~JP5.

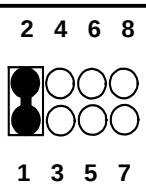
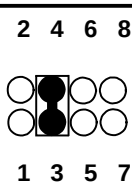
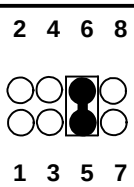
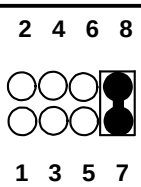
COM2 RS-232/422/485 Select (JP1, JP2~JP5)			
	RS-232*	RS-422	RS-485
JP1			
JP2 JP3 JP4 JP5			

* default

3.10.4 M-Systems DiskOnChip Memory Address Select (JP11)

The M-systems DiskOnChip memory address can be selected by JP11. The choice is D0000~D1FFF, D2000~D3FFF, D4000~D5FFF, D6000~D7FFF.

M-systems DiskOnChip Memory Address Select (JP11)

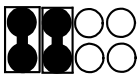
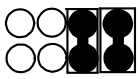
	D0000*	D2000	D4000	D6000
JP11				

* default

3.10.5 Proprietary PCI Bus Master Selection (JP13)

The Proprietary PCI Bus Master is selected by JP13. The choice is Bus Master0 and Bus Master3

Proprietary PCI Bus Master Select (JP13)

	Bus Master 0*	Bus Master 3
JP13		

* default

3.11 Connector Definitions

3.11.1 System Reset Connector (J1)

Signal	PIN
Reset	1
GND	2

3.11.2 External Speaker Connector (J2)

Signal	PIN
SPK	1
NC	2
GND	3
VCC	4

3.11.3 Keyboard Lock & Power Indicator Connector (J3)

Signal	PIN
VCC	1
NC	2
GND	3
Keyboard Inhibit	4
GND	5

3.11.4 Primary IDE / Secondary IDE Active Indicator Connector (J4)

Signal	PIN
VCC	1
HDD Active#	2

3.11.5 Primary IDE Connector (J5)

Signal	PIN		Signal
RESET#	1	2	GND
PDD7	3	4	PDD8
PDD6	5	6	PDD9
PDD5	7	8	PDD10
PDD4	9	10	PDD11
PDD3	11	12	PDD12
PDD2	13	14	PDD13
PDD1	15	16	PDD14
PDD0	17	18	PDD15
GND	19	20	NC
PDDREQ	21	22	GND
PDIOW#	23	24	GND
PDIOR#	25	26	GND
PDIORDY	27	28	GND
PDDACK#	29	30	GND
IRQ14	31	32	NC
PDA1	33	34	NC
PDA0	35	36	PDA2
PDCS1#	37	38	PDCS3#
PDDACT#	39	40	GND

3.11.6 Secondary IDE Connector (J10)

Signal	PIN		Signal
RESET#	1	2	GND
SDD7	3	4	SDD8
SDD6	5	6	SDD9
SDD5	7	8	SDD10
SDD4	9	10	SDD11
SDD3	11	12	SDD12
SDD2	13	14	SDD13
SDD1	15	16	SDD14
SDD0	17	18	SDD15
GND	19	20	NC
SDDREQ	21	22	GND
SDIOW#	23	24	GND
SDIOR#	25	26	GND
SDIORDY	27	28	GND
SDDACK#	29	30	GND
IRQ15	31	32	NC
SDA1	33	34	NC
SDA0	35	36	SDA2
SDCS1#	37	38	SDCS3#
SDDACT#	39	40	GND

3.11.7 Signal Description – Primary & Secondary IDE Connector (J5 & J10)

PDA [2:0]	**Primary Disk Address [2:0].** These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary 0 and Primary 1, these signals are used for the Primary 0 connector.
SDA [2:0]	**Secondary Disk Address [2:0].** These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
PDCS1#	**Primary Disk Chip Select for 1F0H~1F7H Range.** For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
PDCS3#	**Primary Disk Chip Select for 3F0H~3F7H Range.** For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
SDCS1#	**Secondary Chip Select for 170H~177H Range.** For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
SDCS3#	**Secondary Chip Select for 370H~377H Range.** For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
PDD [15:0]	**Primary Disk Data [15:0].** These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
SDD [15:0]	**Secondary Disk Data [15:0].** These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.

PDIOR#	**Primary Disk IO Read.** In normal IDE this is the command to the IDE device that it may drive data onto the PDD [15:0] lines. Data is latched by PIIX4 on the negation edge of PDIOR#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA [2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
SDIOR#	**Secondary Disk IO Read.** In normal IDE mode, this is the command to the IDE device that it may drive data onto the SDD [15:0] lines. Data is latched by the PIIX4 on the negation edge of SDIOR#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA [2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
PDIOW#	**Primary Disk IO Write.** In normal IDE mode, this is the command to the IDE device that it may latch data from the PDD [15:0] lines. Data is latched by the IDE device on the negation edge of PDIOW#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA [2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). For Ultra DMA/33 mode, this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
SDIOW#	**Secondary Disk IO Write.** In normal IDE mode, this is the command to the IDE device that it may latch data from the SDD [15:0] lines. Data is latched by the IDE device on the negation edge of SDIOW#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA [2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In read and write cycles this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.

PDIORDY	**Primary IO Channel Ready.** In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA/33 write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. This is a Schmitt triggered input.
SDIORDY	**Secondary IO Channel Ready.** In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. This is a Schmitt triggered input.
PDDREQ	**Primary Disk DMA Request.** This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
SDDREQ	**Secondary Disk DMA Request.** This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
PDDACK#	**Primary DMA Acknowledge.** This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of PDIOR# or PDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.

SDDACK#	**Secondary DMA Acknowledge.** This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of SDIOR# or SDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
PDDACT#	**Primary Disk Act.** Signal from Primary IDE device indicating Primary IDE device activity. The signal level depends on the hard disk type, normally active low.
SDDACT#	**Secondary Disk Act.** Signal from Secondary IDE device indicating Secondary IDE device activity. The signal level depends on the hard disk type, normally active low.
RESET#	IDE Reset. This signal resets all the devices that are attached to the IDE interface.
IRQ14/15	Interrupt line from hard disk. Connected directly to PC-AT bus.

3.11.8 Floppy Connector (J6)

Signal	PIN		Signal
GND	1	2	DRVDEN0#
GND	3	4	NC
GND	5	6	DRVDEN1#
GND	7	8	INDEX#
GND	9	10	MOA#
GND	11	12	DSB#
GND	13	14	DSA#
GND	15	16	MOB#
GND	17	18	DIR#
GND	19	20	STEP#
GND	21	22	WD#
GND	23	24	WE#
GND	25	26	TRAK0#
GND	27	28	WPT#
GND	29	30	RDATA#
GND	31	32	SIDE1#
GND	33	34	DSKCHG#

3.11.9 Signal Description – Floppy Connector (J6)

RDATA#	The read data input signal from the FDD.
WD#	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
WE#	Write enable. An open drain output.
MOA#	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
MOB#	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.
DSA#	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
DSB#	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.
SIDE1#	This output signal selects side of the disk in the selected drive.
DIR#	Direction of the head step motor. An open drain output Logic 1 = outward motion Logic 0 = inward motion
STEP#	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
DRVDEN0/1#	This output indicates whether a low drive density (250/300kbps at low level) or a high drive density (500/1000kbps at high level) has been selected.
TRAK0#	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track.
INDEX#	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole.
WP#	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected.
DSKCHG#	Diskette change. This signal is active low at power on and whenever the diskette is removed.

3.11.10 ATX Power Button Connector (J8)

Signal	PIN
Power Button Control Signal	1
GND	2

3.11.11 Parallel Port Connector (J11)

Signal	PIN		Signal
STB#	1	2	AFD#
PD0	3	4	ERR#
PD1	5	6	INIT#
PD2	7	8	SLIN#
PD3	9	10	GND
PD4	11	12	GND
PD5	13	14	GND
PD6	15	16	GND
PD7	17	18	GND
ACK#	19	20	GND
BUSY	21	22	GND
PE	23	24	GND
SLCT	25	26	GND

3.11.12 DB25 Parallel Port Connector (J11)

Signal	PIN		Signal
STB#	1		
		14	AFD#
PD0	2		
		15	ERR#
PD1	3		
		16	INIT#
PD2	4		
		17	SLIN#
PD3	5		
		18	GND
PD4	6		
		19	GND
PD5	7		
		20	GND
PD6	8		
		21	GND
PD7	9		
		22	GND
ACK#	10		
		23	GND
BUSY	11		
		24	GND
PE	12		
		25	GND
SLCT	13		

3.11.13 Signal Description – Parallel Port Connector (J11)

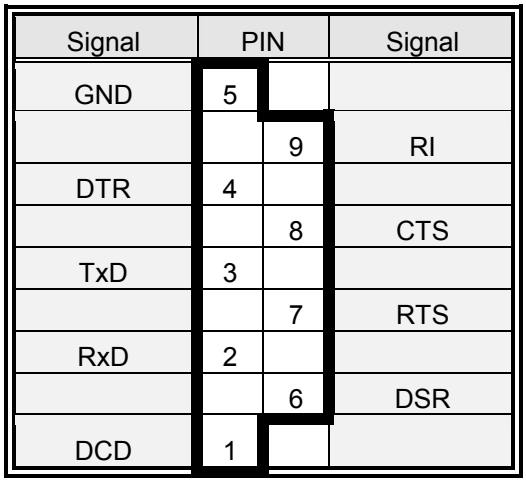
The following signal description covers the signal definitions, when the parallel port is operated in standard centronic mode. The parallel port controller also supports the fast EPP and ECP modes. Please refer to reference 2 for further information.

PD7..0	Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Output line for detection of printer selection. This pin is pulled high internally.
SLCT	An active high input on this pin indicates that the printer is selected. This pin is pulled high internally.
STB#	An active low output is used to latch the parallel data into the printer. This pin is pulled high internally.
BUSY	An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally.
ACK#	An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally.
INIT#	Output line for the printer initialization. This pin is pulled high internally.
AFD#	An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally.
ERR#	An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally.
PE	An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally.

3.11.14 Box Header Serial Port 1 / Serial Port 2 Connector in RS-232 (J9, J12)

Signal	PIN		Signal
DCD	1	2	RxD
TxD	3	4	DTR
GND	5	6	DSR
RTS	7	8	CTS
RI	9	10	NC

3.11.15 Serial Port 1 / Serial Port 2 with External DB9 Connector (J9, J12)



Signal	PIN		Signal
GND	5		
		9	RI
DTR	4		
		8	CTS
TxD	3		
		7	RTS
RxD	2		
		6	DSR
DCD	1		

3.11.16 Signal Description – Serial Port 1 / Serial Port 2 in RS-232 Mode (J9, J12)

TxD	Serial output. This signal sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Serial input. This signal receives serial data from the communication link.
DTR	Data Terminal Ready. This signal indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready. This signal indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send. This signal indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send. This signal indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect. This signal indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator. This signal indicates that the modem has received a telephone ringing signal.

3.11.17 Box Header Serial Port 1 / Serial Port 2 Connector in RS-422 (J9, J12)

Signal	PIN		Signal
NC	10	9	RI
CTS	8	7	RTS
DSR	6	5	GND
TxD+	4	3	TxD-
RxD-	2	1	RxD+

3.11.18 Signal Description – Serial Port 1 / Serial Port 2 in RS-422 Mode (J9, J12)

TxD +/-	Serial output. This differential signal pair sends serial data to the communication link. Data is transferred from Serial Port 2 Transmit Buffer Register to the communication link, if the TxD line driver is enabled through the Serial Port 2's DTR signal. (Modem control register)
RxD +/-	Serial input. This differential signal pair receives serial data from the communication link. Received data is available in Serial Port 2 Receiver Buffer Register.
RTS +/-	Request To Send. The level of this differential signal pair output is controlled through the Serial Port 2's RTS signal (Modem control register).
CTS +/-	Clear To Send. The level of this differential signal pair input could be read from the Serial Port 2's CTS signal. (Modem control register)

3.11.19 Box Header Serial Port 1 / Serial Port 2 Connector in RS-485 (J9, J12)

Signal	PIN		Signal
NC	10	9	CTS/RTS +
NC	8	7	CTS/RTS -
NC	6	5	GND
RxD/TxD +	4	3	RxD/TxD -
NC	2	1	NC

3.11.20 Signal Description – Serial Port 1 / Serial Port 2 in RS-485 Mode (J9, J12)

RxD/TxD +/-	Bi-directional data signal pair. Received data is available in Serial Port 2 Receiver Buffer Register. Data is transferred from Serial Port 2 Transmit Buffer Register to the communication line, if the TxD line driver is enabled through the Serial Port 2's DTR signal (Modem control register). The data transmitted will simultaneously be received the in Serial Port 2 Receiver Buffer Register.
CTS/RTS +/-	Bi-directional control signal pair. The level of this differential signal pair could be read from the Serial Port 1's CTS signal (Modem control register). The level of this differential signal pair could be controlled through the Serial Port 2's RTS signal (Modem control register).

Warning: Do not select a mode different from the one used by the connected peripheral, as this may damage CPU board and/or peripheral.

The transmitter drivers in the port are short circuit protected by a thermal protection circuit. The circuit disables the drivers when the die temperature reach 150 °C.

RS-422 mode is typically used in point to point communication. Data and control signal pairs should be terminated in the receiver end with a resistor matching the cable impedance (typ. 100-120 Ω). The resistors could be placed in the connector housing.

RS-485 mode is typically used in multi drop applications, where more than 2 units are communicating. The data and control signal pairs should be terminated in each end of the communication line with a resistor matching the cable impedance (typical 100-120 Ω). Stubs to substations should be avoided.

3.11.21 USB Connector (J13, J19)

Signal	PIN CH2	PIN CH1	Signal
NC	9	10	VCC2
GND	7	8	D2-
D1+	5	6	D2+
D1-	3	4	GND
VCC1	1	2	NC

3.11.22 Signal Description – USB Connector (J13, J19)

D1+ / D1-	Differential bi-directional data signal for USB channel 0. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs.
D2+ / D2-	Differential bi-directional data signal for USB channel 1. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs.
VCC	5 V DC supply for external devices. Maximum load according to USB standard.

3.11.23 CPU Fan and System Fan Connector (J14, J25)

Signal	PIN
GND	1
+12V	2
TAC	3

3.11.24 Fast & Standard IrDA Connector (J15)

Signal	PIN
+5V	1
FIR	2
IRRX	3
GND	4
IRTX	5
Over Current Off	6

3.11.25 Signal Configuration – Fast & Standard IrDA Connector (J15)

IRRX	Infrared Receiver input
IRTX	Infrared Transmitter output

3.11.26 ATX Power Controller (J16)

Signal	PIN
Power Good	1
5V Stand-by	2
Power On	3
GND	4

3.11.27 Smart Card Interface (J17)

Signal	PIN CH2	PIN CH1	Signal
NC	13	14	NC
GND	11	12	SCRPRES#
NC	9	10	SCRIO
SCRCLK	7	8	NC
SCRPFET#	5	6	SCRRST
NC	3	4	NC
VCC1	1	2	NC

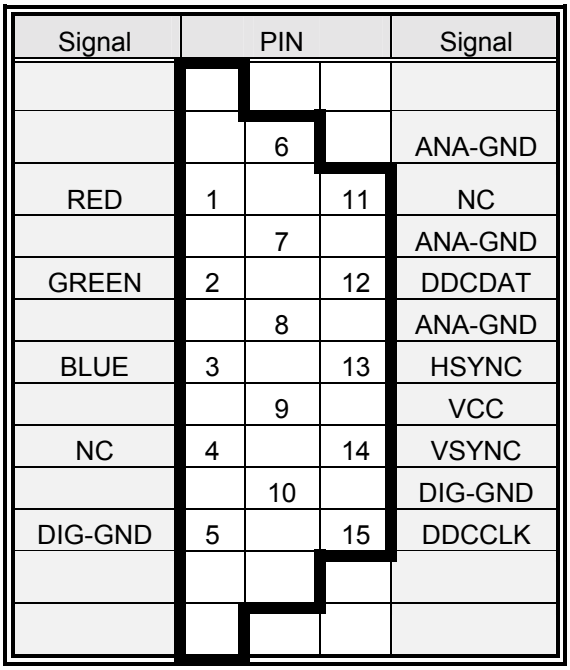
3.11.28 10/100 BASE-Tx Ethernet Connector (J18, J20)

Signal	PIN
TXD+	1
TXD-	2
RXD+	3
NC	4
NC	5
RXD-	6
NC	7
NC	8

3.11.29 Signal Description – 10/100Base-Tx Ethernet Connector (J18, J20)

TXD+ / TXD-	Ethernet 10/100Base-Tx differential transmitter outputs.
RXD+ / RXD-	Ethernet 10/100Base-Tx differential receiver inputs.

3.11.30 CRT Connector (J22)



Signal	PIN			Signal
		6		ANA-GND
RED	1		11	NC
		7		ANA-GND
GREEN	2		12	DDCDAT
		8		ANA-GND
BLUE	3		13	HSYNC
		9		VCC
NC	4		14	VSYNC
		10		DIG-GND
DIG-GND	5		15	DDCCLK

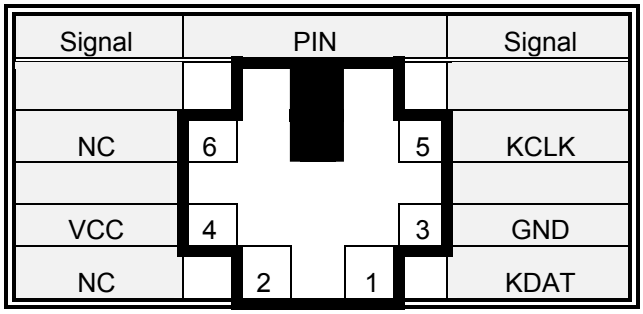
3.11.31 Signal Description – CRT Connector (J22)

HSYNC	CRT horizontal synchronisation output.
VSYNC	CRT vertical synchronisation output.
DDCCLK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.
DDCDAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
RED	Analog output carrying the red colour signal to the CRT. For 75 Ω cable impedance.
GREEN	Analog output carrying the green colour signal to the CRT. For 75 Ω cable impedance.
BLUE	Analog output carrying the blue colour signal to the CRT. For 75 Ω cable impedance.
DIG-GND	Ground reference for HSYNC and VSYNC.
ANA-GND	Ground reference for RED, GREEN, and BLUE.

3.11.32 Internal Keyboard Connector (J24)

Signal	PIN
KCLK	1
KDAT	2
NC	3
GND	4
VCC	5

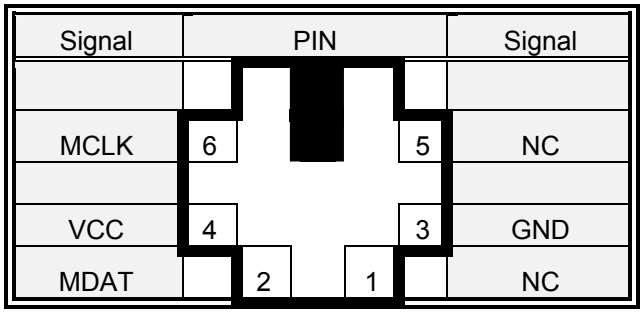
3.11.33 PS/2 Keyboard Connector (J26)



3.11.34 Signal Description – Int. & PS/2 Keyboard Connector (J24, J26)

KCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.

3.11.35 PS/2 Mouse Connector (J26)



3.11.36 Signal Description – PS/2 Mouse Connector (J26)

MCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.

3.11.37 Proprietary PCI Connector (J21)

Signal	PIN		Signal
+12V	1	2	AGND
+12V	3	4	AGND
VSYNC	5	6	RED
GND	7	8	GREEN
HSYNC	9	10	BLUE
CLK	11	12	GND
GND	13	14	PIRQ#
REQ#	15	16	GNT#
AD31	17	18	RST#
AD29	19	20	+3.3V
DEVSEL#	21	22	+3.3V
AD27	23	24	AD30
AD25	25	26	AD28
C/BE3#	27	28	GND
+3.3V	29	30	AD26
+3.3V	31	32	AD24
AD23	33	34	IDSEL
AD21	35	36	AD22
AD19	37	38	AD20
GND	39	40	GND
AD17	41	42	AD18
C/BE2#	43	44	AD16
IRDY#	45	46	FRAME#
PERR#	47	48	TRDY#
SERR#	49	50	PAR
C/BE1#	51	52	STOP#
AD14	53	54	AD15
AD12	55	56	AD13
GND	57	58	AD11
AD10	59	60	LOCK#
AD8	61	62	AD9
GND	63	64	C/BE0#
AD7	65	66	AD6
AD5	67	68	AD4
AD3	69	70	GND
AD1	71	72	AD2
+5V	73	74	AD0
+5V	75	76	GND
+5V	77	78	+3.3V
+5V	79	80	+3.3V

3.11.38 Signal Description – Proprietary PCI Connector (J21)

3.11.38.1 Address & Data

AD [31::00]	*Address* and *Data* are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which **FRAME#** is asserted. During the address phase **AD [31::00]** contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases **AD [07::00]** contain the least significant byte (lsb) and **AD [31::24]** contain the most significant byte (msb). Write data is stable and valid when **IRDY#** is asserted and read data is stable and valid when **TRDY#** is asserted. Data is transferred during those clocks where both **IRDY#** and **TRDY#** are asserted.
C/BE [3::0]**#**	*Bus Command* and *Byte Enables* are multiplexed on the same PCI pins. During the address phase of a transaction, **C/BE [3::0]#** define the bus command. During the data phase **C/BE [3::0]#** are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. **C/BE[0]#** applies to byte 0 (lsb) and **C/BE[3]#** applies to byte 3 (msb).
PAR	*Parity* is even parity across **AD [31::00]** and **C/BE [3::0]#**. Parity generation is required by all PCI agents. **PAR** is stable and valid one clock after the address phase. For data phases, **PAR** is stable and valid one clock after either **IRDY#** is asserted on a write transaction or **TRDY#** is asserted on a read transaction. Once **PAR** is valid, it remains valid until one clock after the completion of the current data phase. (**PAR** has the same timing as **AD[31::00**], but it is delayed by one clock.) The master drives **PAR** for address and write data phases; the target drives **PAR** for read data phases.

3.11.38.2 System

CLK	*Clock* provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except **RST#**, **INTA#**, **INTB#**, **INTC#**, and **INTD#**, are sampled on the rising edge of **CLK** and all other timing parameters are defined with respect to this edge. PCI operates up to 33 MHz or 66 MHz and, in general, the minimum frequency is DC (0 Hz).
RST#	*Reset* is used to bring PCI-specific registers, sequencers, and signals to a consistent state. What effect **RST#** has on a device beyond the PCI sequencer is beyond the scope of this specification, except for reset states of required PCI configuration registers. Anytime **RST#** is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated. **SERR#** (open drain) is floated. **REQ#** and **GNT#** must both be tri-stated (they cannot be driven low or high during reset). To prevent **AD**, **C/BE#**, and **PAR** signals from floating during reset, the central resource may drive these lines during reset (bus parking) but only to a logic low level–they may not be driven high. **RST#** may be asynchronous to **CLK** when asserted or deasserted. Although asynchronous, deassertion is guaranteed to be a clean, bounce-free edge. Except for configuration accesses, only devices that are required to boot the system will respond after reset.

3.11.38.3 Interface Control

FRAME#	*Cycle Frame* is driven by the current master to indicate the beginning and duration of an access. **FRAME#** is asserted to indicate a bus transaction is beginning. While **FRAME#** is asserted, data transfers continue. When **FRAME#** is deasserted, the transaction is in the final data phase or has completed.
IRDY#	*Initiator Ready* indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. **IRDY#** is used in conjunction with **TRDY#**. A data phase is completed on any clock both **IRDY#** and **TRDY#** are sampled asserted. During a write, **IRDY#** indicates that valid data is present on **AD [31::00**]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both **IRDY#** and **TRDY#** are asserted together.
TRDY#	*Target Ready* indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. **TRDY#** is used in conjunction with **IRDY#**. A data phase is completed on any clock both **TRDY#** and **IRDY#** are sampled asserted. During a read, **TRDY#** indicates that valid data is present on **AD [31::00**]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both **IRDY#** and **TRDY#** are asserted together.
STOP#	*Stop* indicates the current target is requesting the master to stop the current transaction.
LOCK#	*Lock* indicates an atomic operation that may require multiple transactions to complete. When **LOCK#** is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of **LOCK#**. Control of **LOCK#** is obtained under its own protocol in conjunction with **GNT#**. It is possible for different agents to use PCI while a single master retains ownership of **LOCK#**. If a device implements Executable Memory, it should also implement **LOCK#** and guarantee complete access exclusion in that memory. A target of an access that supports **LOCK#** must provide exclusion to a minimum of 16 bytes (aligned). Host bridges that have system memory behind them should implement **LOCK#** as a target from the PCI bus point of view and optionally as a master.
IDSEL	*Initialization Device Select* is used as a chip select during configuration read and write transactions.
DEVSEL#	*Device Selec*t, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, **DEVSEL#** indicates whether any device on the bus has been selected.

3.11.38.4 Arbitration

REQ#	*Request* indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own **REQ#** which must be tri-stated while **RST#** is asserted.
GNT#	*Grant* indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own **GNT#** which must be ignored while **RST#** is asserted.

3.11.38.5 Error Reporting

PERR#	*Parity Error* is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The **PERR#** pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of **PERR#** is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the **PERR#** signal will be asserted for more than a single clock.) **PERR#** must be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a **PERR#** until it has claimed the access by asserting **DEVSEL#** (for a target) and completed a data phase or is the master of the current transaction.
SERR#	*System Error* is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required. **SERR#** is pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of **SERR#** is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of **SERR#** to the deasserted state is accomplished by a weak pullup (same value as used for s/t/s) which is provided by the system designer and not by the signaling agent or central resource. This pullup may take two to three clock periods to fully restore **SERR#**. The agent that reports **SERR#**s to the operating system does so anytime **SERR#** is sampled asserted.

3.11.38.6 Interrupts

PIRQ#	Interrupts on PCI are optional and defined as "level sensitive," asserted low (negative true), using open drain output drivers. The assertion and deassertion of **INTx#** is asynchronous to **CLK**. A device asserts its **INTx#** line when requesting attention from its device driver. Once the **INTx#** signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device deasserts its **INTx#** signal. PCI defines one interrupt line for a single function device and up to four interrupt lines for a *multi-function* 7 device or connector. For a single function device, only **INTA#** may be used while the other three interrupt lines have no meaning. **PIRQ#** is connected to **INTB#**

4. AMI BIOS Setup

ECB-865 is equipped with the AMI BIOS stored in Flash ROM. This BIOS has a built-in Setup program that allow users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods.

4.1 Entering Setup

Turn on or reboot the computer. When the message "Hit<DEL>" appears if you want to run SETUP, press <DEL> key immediately to enter BIOS Setup program.

If the message disappears before you respond, but you still wish to enter Setup please restart the system to try "COLD START" again by turning the system OFF and then ON, or touch the "RESET" button. You may also restart from "WARM START" by pressing <Ctrl>, <Alt>, and <Del> keys simultaneously. If you do not press these keys at the right time and the system will not boot, an error message will be displayed and you will again be asked to,

```
Press <F1> to Run SETUP or Resume
```

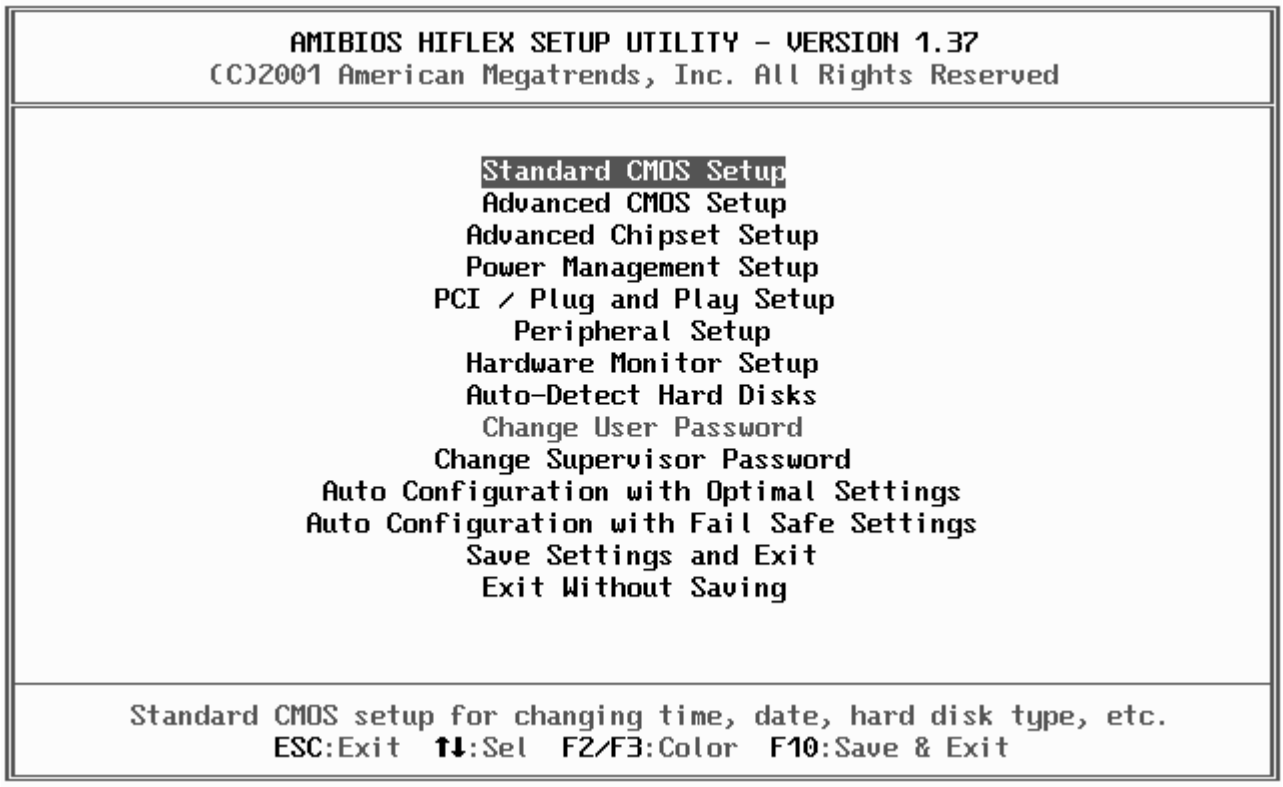
In HIFLEX BIOS Setup, you can use the keyboard to choose among options or modify the system parameters to match the options with yours system. The table below will show you all of keystroke functions in BIOS Setup.

Editing Keys	Function
<Tab>	Move to the next field
←↑→↓	Move the next field to the left, above, right, or below
<Enter>	Select in the current field
+ / -	Increments /Decrements a value
<Esc>	Close the current operation and return to previous level
<PgUp>	Returns to the previous option
<PgDn>	Advances to the next option
<F2>/<F3>	Select background color
<F10>	Show "Save current settings and exit(Y/N)" in main menu

4.2 AMI BIOS Setup Main Menu

Once you enter ECB-865 AMI BIOS COMS Setup Utility, the Main Menu “Standard CMOS Setup” will appear on the screen. The Main Menu allows you to select from eleven Setup functions and two exit choices. Use arrow keys to switch the items and press

<Enter> key to accept or enter the sub-menu


AMIBIOS HIFLEX SETUP UTILITY - VERSION 1.37
(C)2001 American Megatrends, Inc. All Rights Reserved
Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Power Management Setup
PCI / Plug and Play Setup
Peripheral Setup
Hardware Monitor Setup
Auto-Detect Hard Disks
Change User Password
Change Supervisor Password
Auto Configuration with Optimal Settings
Auto Configuration with Fail Safe Settings
Save Settings and Exit
Exit Without Saving
Standard CMOS setup for changing time, date, hard disk type, etc.
ESC:Exit ↑↓:Sel F2/F3:Color F10:Save & Exit

Note:

It is strongly recommended to reload Optimal setting if CMOS is lost or BIOS is updated.

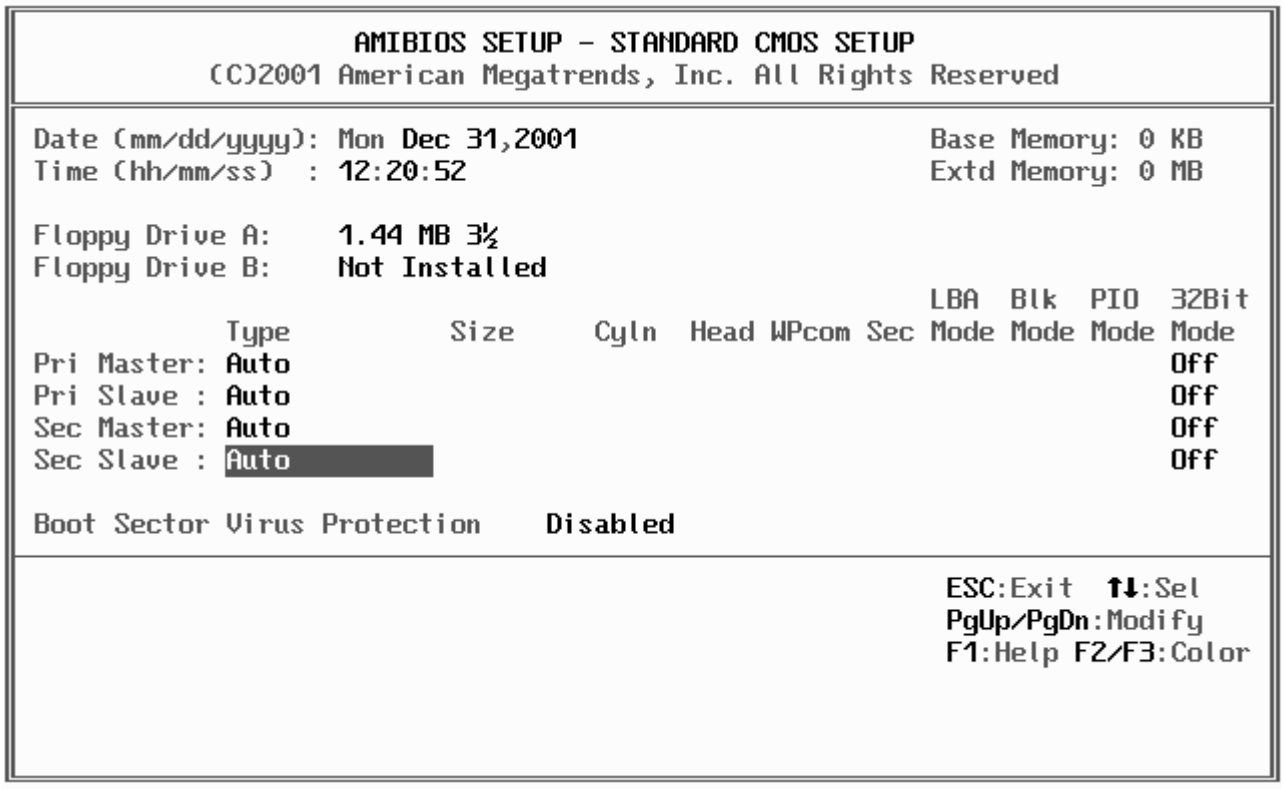
4.3 CMOS Setup Reference Table

This Setup reference table includes all the Optimal, Failsafe, and other options setting in each BIOS setup item. It is very easy to take a look for crossing reference. If you want to go details, you can directly refer to item description in sub-section.

4.3.1 Standard CMOS Setup Menu

This Setup page includes all the items in standard CMOS Setup. Use the arrow keys to highlight the item and then use the <PgUp>/<PgDn> or <+>/<-> keys to select the value or number you want in each item and press <Enter> key to certify it.

Follow command keys in CMOS Setup table to change **Date**, **Time**, **Drive type**, and Boot Sector Virus Protection Status.


AMIBIOS SETUP - STANDARD CMOS SETUP
(C)2001 American Megatrends, Inc. All Rights Reserved
Date (mm/dd/yyyy): Mon Dec 31,2001
Time (hh/mm/ss) : 12:20:52
Base Memory: 0 KB
Extd Memory: 0 MB
Floppy Drive A: 1.44 MB 3½
Floppy Drive B: Not Installed
Type Size Cyln Head WPcom Sec LBA Mode Blk Mode PIO Mode 32Bit Mode
Pri Master: Auto Off
Pri Slave : Auto Off
Sec Master: Auto Off
Sec Slave : Auto Off
Boot Sector Virus Protection Disabled
ESC:Exit ↑↓:Sel
PgUp/PgDn:Modify
F1:Help F2/F3:Color

4.3.1.1 Date and Time Configuration

Select the Date and Time icon in the Standard CMOS setup. The current values for each category are displayed. Enter new values through the keyboard or hit the "+" or "-" key to change values.

4.3.1.2 Floppy A, Floppy B

Select the appropriate specifications to configure the type of floppy drive that is attached to the system: 360 KB 5¼", 1.2 MB 5¼", 720 KB 3½", and/or 1.44 MB 3½". The settings have not been pre-installed.

4.3.1.3 Master Disk, Slave Disk

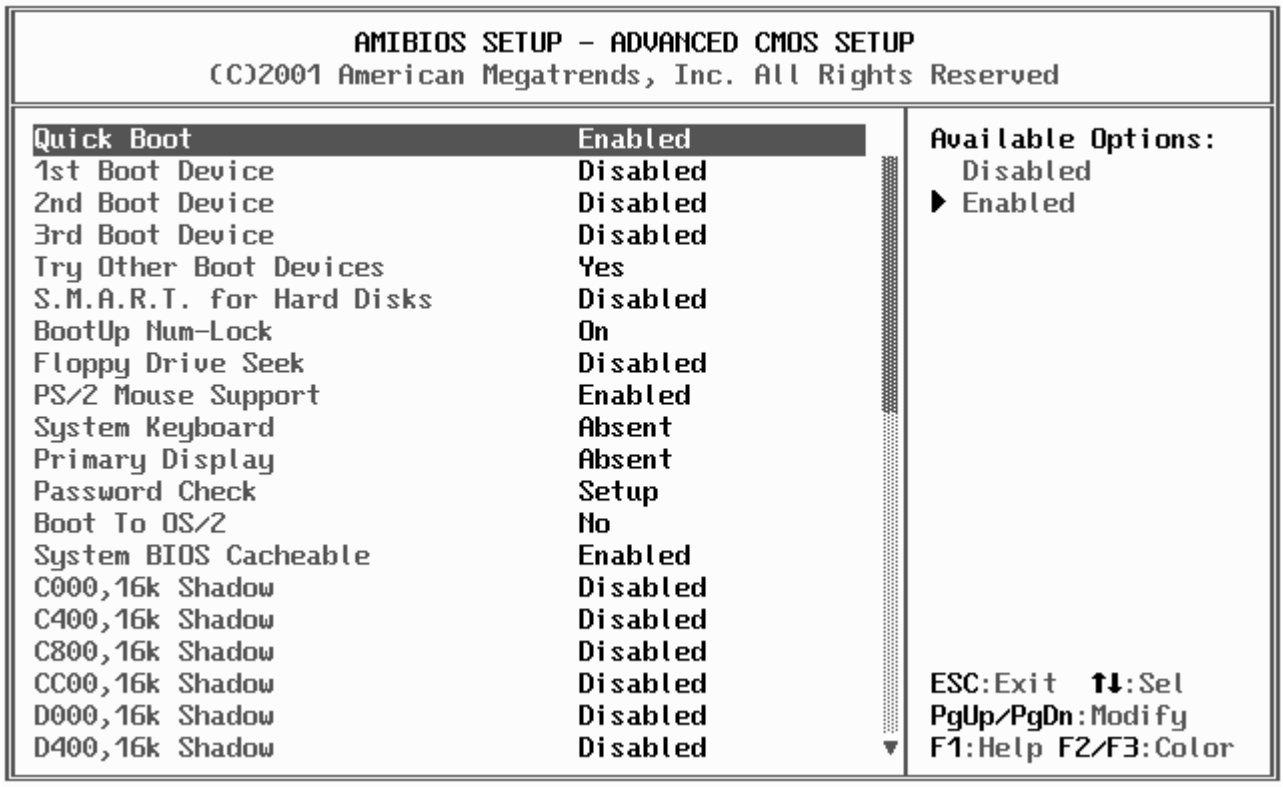
Select the appropriate values to configure the hard disk type you are using for the master and the slave. Available types are *1~4*6, *US*ER, *AUT*O, *Not Installe*d, and *CDRO*M. The settings have not been preinstalled.

4.3.1.4 Boot Sector Virus Protection

Enabling this option allows the system to issue a warning when any program (or virus) issues a disk format command or attempts to write to the boot sector of the hard disk drive. Further confirmation is required before accessing this particular section of the hard disk drive.

4.3.2 Advanced CMOS Setup Defaults

This Setup includes all of the advanced features in the system. The detail descriptions are specified as below.



4.3.2.1 Quick Boot

Set this option to *Enabled* to instruct AMIBIOS to boot quickly when the computer is powered on.

Disabled: AMIBIOS tests all system memory. AMIBIOS waits up to 40seconds for a READY signal from the IDE hard disk drive. AMIBIOS waits for 0.5 seconds after sending a RESET signal to the IDE drive to allow the IDE drive time to get ready again. AMIBIOS checks for a <Del> key press and runs AMIBIOS Setup if the key has been pressed.

Enabled: AMIBIOS does not test system memory above 1 MB. AMIBIOS does not wait up to 40 seconds for a READY signal from the IDE hard disk drive. If a READY signal is not received immediately from the IDE drive, AMIBIOS does not configure that drive. AMIBIOS does not wait for 0.5 seconds after sending a RESET signal to the IDE drive to allow the IDE drive time to get ready again. You cannot run AMIBIOS Setup at system boot, because there is no delay for the Hit <Del> to run Setup message.

4.3.2.2 1st / 2nd / 3rd Boot Device

These options determine the sequence of boot drives (floppy drive A:, hard disk drive C:, or CD-ROM drive) that the AMIBIOS attempts to boot from after AMIBIOS POST completes.

4.3.2.3 Try Other Boot Device

Set this option to *Yes* to try other boot device. The settings are *Yes* or *No.* The default setting is *Yes*.

4.3.2.4 S.M.A.R.T. for Hard Disks

Set this option to *Enabled* the S.M.A.R.T function for Hard Disks. The settings are *Enabled* or *Disable*d. The default setting is *Disable*d.

4.3.2.5 BootUp Num-Lock

Set this option to *Off* to turn the Num Lock key off when the computer is booted so you can use the arrow keys on both the numeric keypad and the keyboard. The settings are *On* or *Off.* The default setting is *On*.

4.3.2.6 Floppy Drive Swap

Set this option to *Enabled* to permit drives A: or B: to be swapped. The settings are *Enabled* or *Disable*d. The default setting is *Disable*d.

4.3.2.7 Floppy Drive Seek

Set this option to *Enabled* to specify that floppy drive A: will perform a seek operation at system boot. The settings are *Enabled* or *Disabled.* The default setting is *Disabled.*

4.3.2.8 PS/2 Mouse Support

When this option is set to *Enable*d, AMIBIOS supports a PS/2-type mouse. The settings are *Enabled* or *Disabled.* The default setting is *Enabled.*

4.3.2.9 Primary Display

This option specifies the type of display monitor and adapter in the computer. The settings are *Mono*, *CGA40x25, CGA80x25, VGA/EGA,* or *Absent.* The default setting is V*GA/EGA.*

4.3.2.10 Password Check

This option enables the password checking when the system boots up or runs CMOS Setup. It only takes effect after setting Change Supervisor Password.

Setup: This option will force system to check password before running Setup if you have already entered the current user password in “Change User Password”. By that time, the system will be only able to boot but deny accessing Setup.

Always: Password prompt appears every boot-up. The system will not boot and deny access Setup with invalid password. The best way is to clear CMOS or try to reload BIOS Setup to boot up system.

4.3.2.11 Boot To OS/2

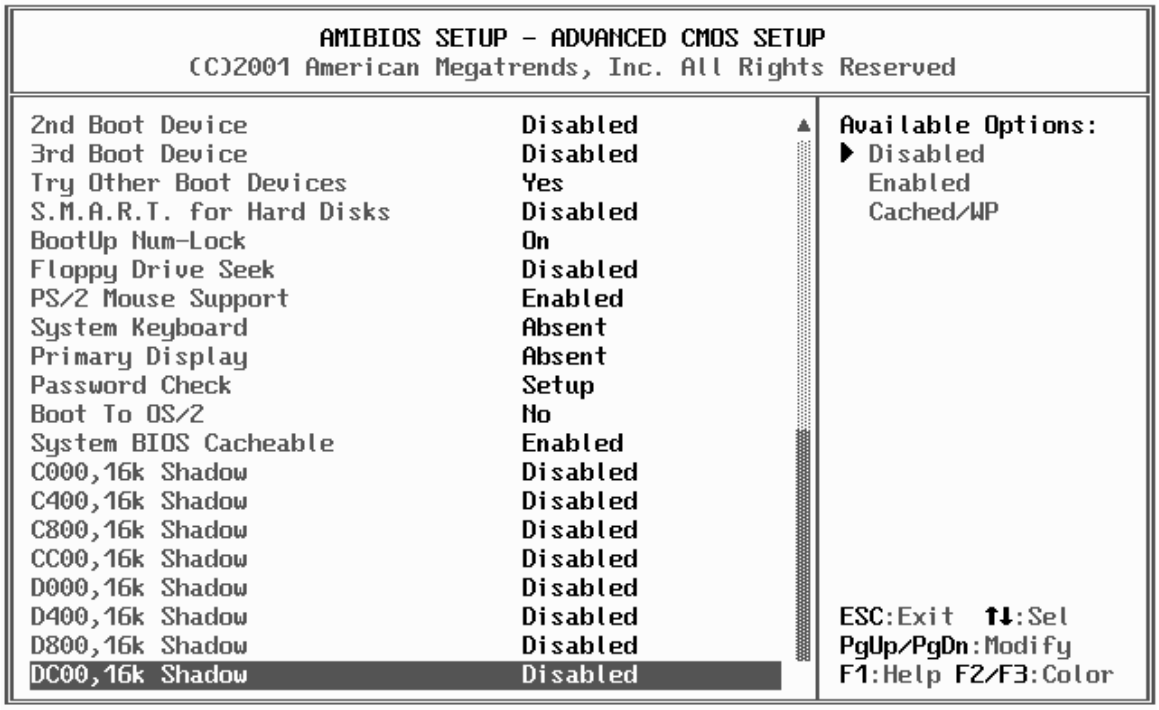
Set this option to *Yes* to permit AMIBIOS to run with IBM OS/2. The settings are *Yes* or *No.* The default setting is *No.*

4.3.2.12 System BIOS Cacheable

When this option is set to *Enabled,* the contents of the F0000h system memory segment can be read from or written to L2 cache memory. The contents of the F0000h memory segment are always copied from the BIOS ROM to system RAM for faster execution. The settings are *Enabled* or *Disabled.*

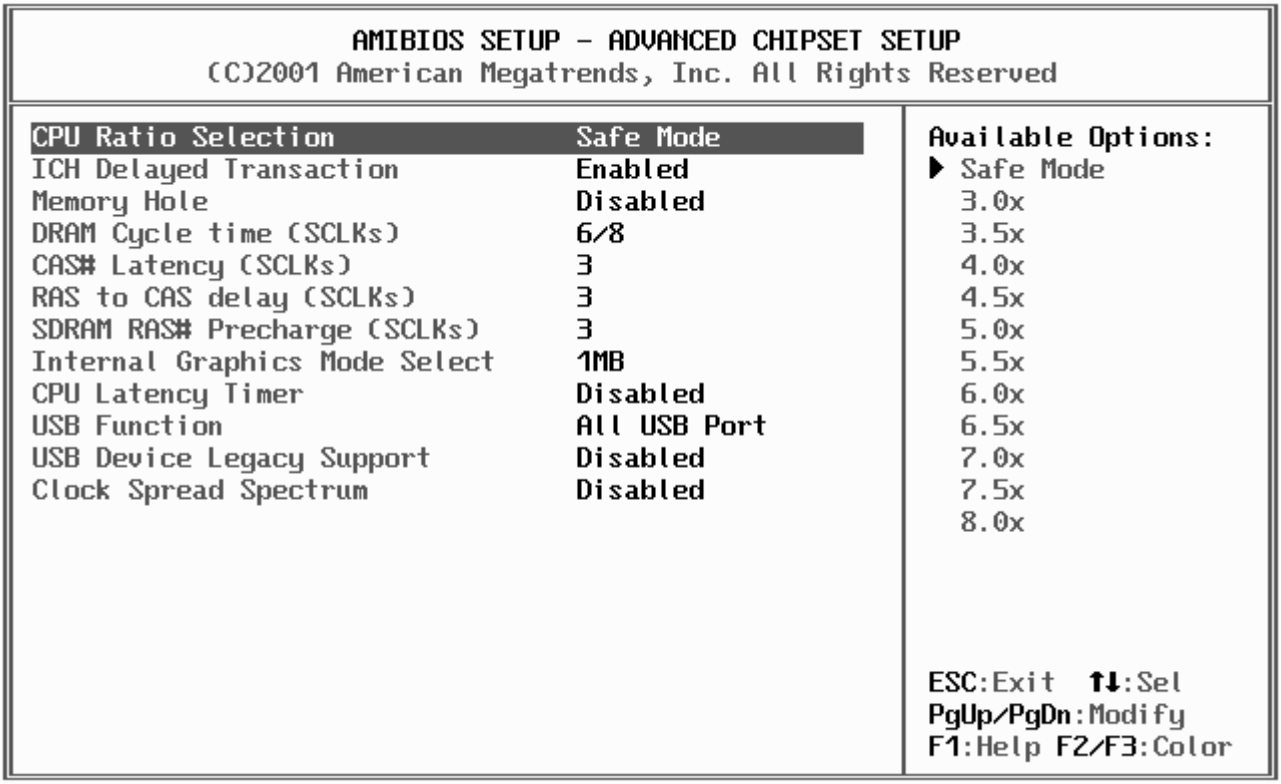
4.3.2.13 Shadow Memory (from Address C000~DFFF, 16K Per Segment)

Each of segments provides three options "Disabled", "Enabled", and "Cached" for faster adapter's ROM execution. However this shadow function is Chipset oriented and dependent on system hardware feature. In general, C000 and C800 will be allocated for VGA BIOS and set to *Cached* to get higher display performance by shadowing and caching feature. If user chooses *Enabled* setting, only BIOS shadow function is active.



4.3.3 Advanced Chipset Setup Defaults

This Setup is very important to keep system's stability. If you are not technical person, do not attempt to change any parameters. The best way is to choose optimal default setting.



4.3.3.1 CPU Ratio Selection

This option provides different CPU clock Ratios from 3.0x to 8.0x. When you change the ratio, the overall CPU speed will change accordingly. In the default setting of "Safe Mode", the CPU operates its own original clock rate automatically.

Note:

> It is strongly recommended to set the default setting of " Safe Mode". Selecting the higher CPU clock rate may get higher CPU speed, but it will cause the system unstable, the damages of the system, and even burning the CPU!

4.3.3.2 ICH Delayed Transaction

ICH2 equips an embedded 32-bit post write buffer to support system delay transaction cycles. This option provides the compliance with PCI specification version 2.1 devices.

4.3.3.3 Memory Hole

This option allows the end user to specify the location of a memory hole for memory space requirement from ISA-bus cards.

4.3.3.4 DRAM Cycle time (SCLKs)

This option selects the number of SCLKs for an access cycle.

4.3.3.5 CAS# Latency (SCLKs)

This option controls the number of SCLKs between the time a read command is sampled by the SDRAM and GMCH 82815E samples corresponding data from the SDRAMs.

4.3.3.6 SDRAM RAS# to CAS# Delay

This option controls the number of SCLKs (SDRAM Clock) from a row activate command to a read or write command. If your system installs good quality of SDRAM, you can set this option to "2 SCLKs" to obtain better memory performance. Normally, the option will be set to "*3 SCLKs*".

4.3.3.7 SDRAM RAS# Precharge

This option controls the number of SCLKs for RAS# precharge. If your system installs good quality of SDRAM, you can set this option to "2 SCLKs" to obtain better memory performance.

4.3.3.8 Internal Graphic Mode Select

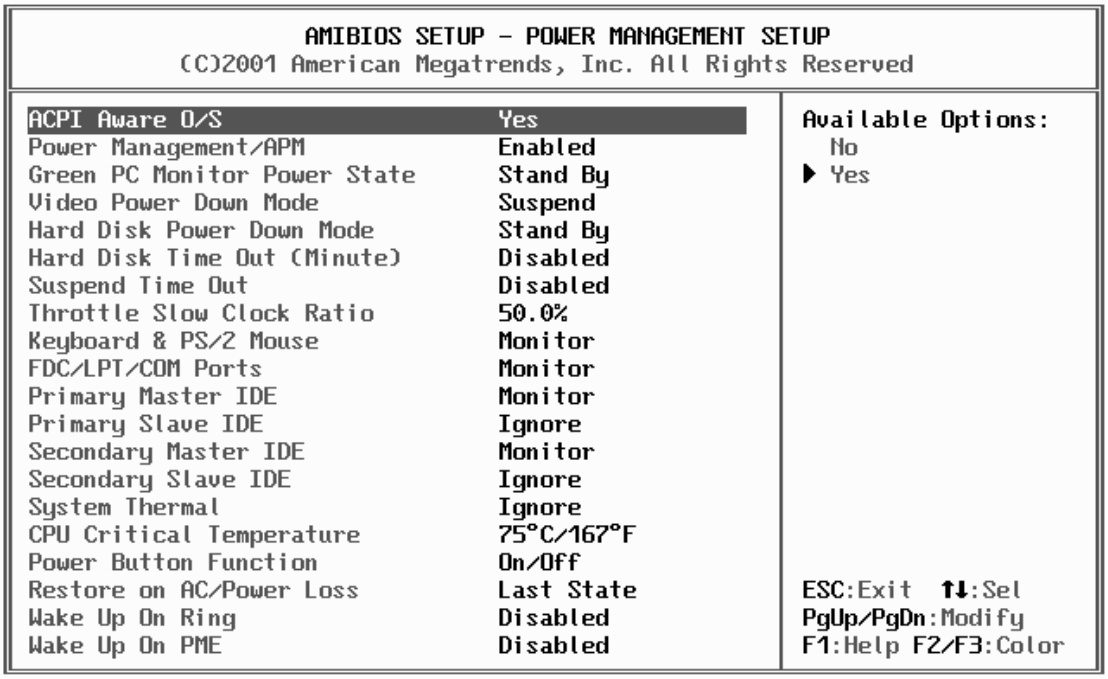
This option allows the end users to specify the size of video memory shared from system memory.

4.3.3.9 USB Function

This option will enable on-chip USB function to support USB (Universal Serial Bus) peripheral devices if user chooses the "Enabled" setting.

4.3.4 Power Management Setup Defaults

This APM (Advanced Power Management) determines how much power energy setting below items to handle system power resource can save. The following descriptions will specify the definition of each item in details.


AMIBIOS SETUP - POWER MANAGEMENT SETUP
(C)2001 American Megatrends, Inc. All Rights Reserved
ACPI Aware O/S Yes
Power Management/APM Enabled
Green PC Monitor Power State Stand By
Video Power Down Mode Suspend
Hard Disk Power Down Mode Stand By
Hard Disk Time Out (Minute) Disabled
Suspend Time Out Disabled
Throttle Slow Clock Ratio 50.0%
Keyboard & PS/2 Mouse Monitor
FDC/LPT/COM Ports Monitor
Primary Master IDE Monitor
Primary Slave IDE Ignore
Secondary Master IDE Monitor
Secondary Slave IDE Ignore
System Thermal Ignore
CPU Critical Temperature 75°C/167°F
Power Button Function On/Off
Restore on AC/Power Loss Last State
Wake Up On Ring Disabled
Wake Up On PME Disabled
Available Options:
No
Yes
ESC:Exit ↑↓:Sel
PgUp/PgDn:Modify
F1:Help F2/F3:Color

4.3.4.1 ACPI Aware O/S

This item allows you to *enable*/*disable* the Advanced Configuration and Power Management (ACPI).

The choice: *Yes*, *No*.

4.3.4.2 Power Management/ APM

This item allows you to *enable*/*disable* the Power Management and the Advanced Power Management functions in following items. If you set this function to *disable,* the following items in this page will become to dark grey color and can't be selectable.

4.3.4.3 Green PC Monitor Power State

This option is used to decide what kind of power states is effective. There are three options "Stand By", "Suspend", and "Off" in this feature. The "Stand By" option is to turn off light power by handling of Monitor signals. The other "Suspend" mode is to turn off heavy power. And the other one, "Off" state, is really to turn off the power of the monitor.

4.3.4.4 Stand by Time Out (Minute)

This option specifies the length of the period of system inactivity while the computer is in Full-On power state before the computer is placed in Standby mode. When this length of time expires, the computer enters Standby Timeout state. In Standby mode, some power use is curtailed.

4.3.4.5 Suspend Time Out (Minute)

This option is the same as **Stand by Time out** function. These two features will be enabled to monitor power of sub-items "Display Activity", "Serial port", "Parallel Port", "Floppy", "Pri-HDD", and "Sec-HDD" independently. It is also used to control CPU throttle running function. All of sub-items will be ineffective in selection of disabling "Stand by Time out" or "Suspend Time out" even if it can be choused by user in BIOS setup menu.

4.3.4.6 Throttle Slow Clock Ratio

This option specifies the speed at which the system clock runs in power saving modes. The settings are expressed as duty cycle of the STPCLK# signal. This duty cycle indicates the percentage of time the STPCLK# signal is asserted while in the throttle mode.

4.3.4.7 System Thermal

Set this option to *Monitor* for CPU thermal monitoring and speed down control. The system will automatically supervise the CPU environmental temperature. If the CPU surface temperature reaches the trip point set in Hardware Monitor Setup, the thermal detection will be effective and CPU will run in throttle control manner. The overall system performance will be reduced to half. This option is a trade-off of system performance and stability and configurable by user. The default setting is *Ignore*. You can choose *Monitor* setting to enable this thermal function.

4.3.4.8 Thermal Slow Clock Ratio

This option specifies the speed at which the system clock runs in thermal trip point. The settings are expressed as duty cycle of the STPCLK# signal. This duty cycle indicates the percentage of time the STPCLK# signal is asserted while in the over heat mode.

4.3.4.9 CPU Critical Temperature

Set this option to monitor CPU thermal trip point defined by user. If the System Thermal option in CMOS setup is set to "Monitor" state and CPU surface temperature is over this critical temperature, the system will automatically enter speed down mode.

4.3.4.10 Power Button Function

This item is used to handle soft power on/off regardless of time counting (generally speaking, it is 4 sec) if you set it to *On/Off*. You can easily power on/off system by pressing power button (toggle switch) directly. This feature is only available on system with ATX power control interface. If you use standard AT power supply, this option will be ignored. However choose the "Suspend" setting, system will be forced into suspend mode when user turn it off unless you can consecutively press the power button for more than 4 second to get in Soft off function.

4.3.4.11 Wake Up on Ring

This item will be used to wake up system from remote ringing control under Soft Off condition. If you choose "Disabled" setting, the system will be not resumed by modem ring.

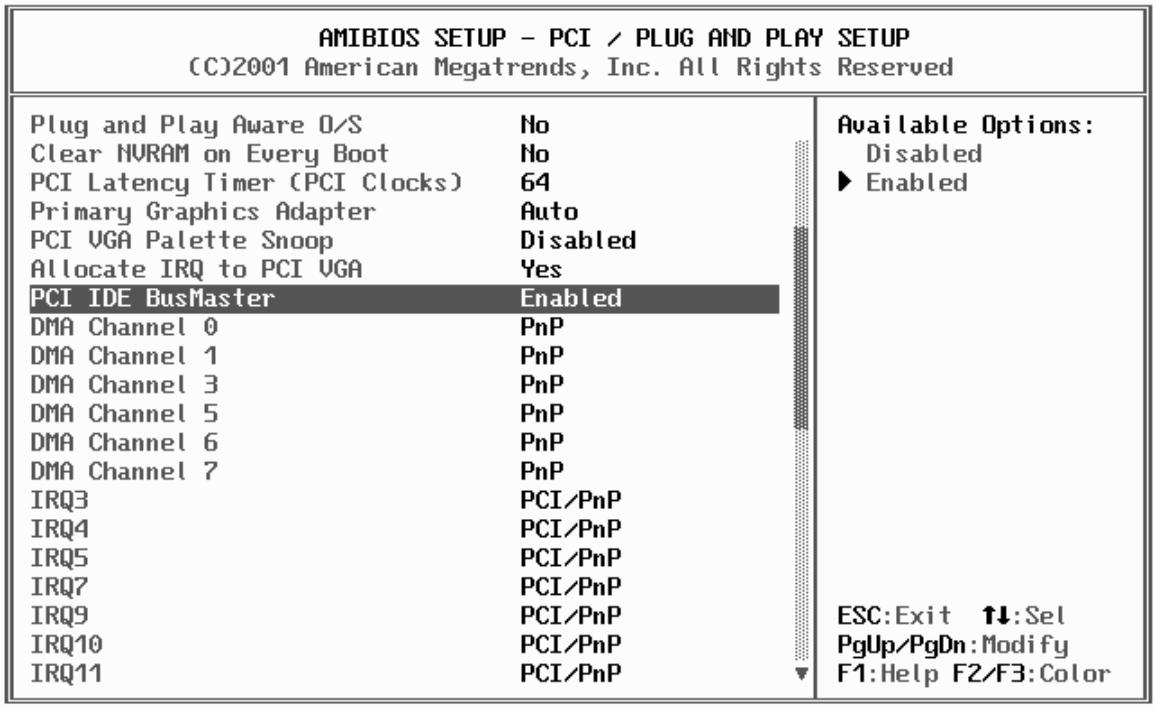
4.3.4.12 Wake Up on LAN

This item will be used to wake up system from remote Network control under Soft Off condition. If you choose "Disabled" setting, the system will be not resumed by LAN start.

4.3.5 PCI / Plug and Play Setup Defaults

This section describes configuring the PCI bus system. PCI (Peripheral Component Interconnect) is a system that allows I/O devices to operate at speeds nearing CPU's when they communicate with own special components.

All of options described in this section are important and technical and it is strongly recommended that only experienced users could make any changes to the default settings.



4.3.5.1 Plug and Play Aware O/S

Set this option to "Yes" if the operating system installed in the computer is Plug and Play-aware. BIOS only detects and enables PnP ISA adapter cards that are required for system boot. The Windows 95 operating system detects and enables all other PnP-aware adapter cards. Windows 95 is PnP-aware. Set this option to "No" if the operating system (such as DOS, OS/2, Windows 3.x) does not use PnP.

Note:

You must set this option correctly, or PnP-aware adapter cards installed in your computer will not be configured properly.

4.3.5.2 Clear NVRAM

This option is used to clear NVRAM and check or update ESCD (Extended System Configuration Data) data after system power on. Set this option to *No* that will not clear NVRAM and the operation of update ESCD is effective in different ESCD data comparison. If you select the "Yes" setting, then the BIOS will update ESCD each time of power on.

4.3.5.3 PCI Latency Timer (PCI Clocks)

This option sets the latency of all PCI devices on the PCI bus. The settings are in units equal to PCI clocks. The settings are *32, 64, 96, 128, 160, 192, 224,* or *248.* The Optimal and Fail-Safe default settings are *6*4.

4.3.5.4 PCI / VGA Palette Snoop

Leave this field at *Disabled*.

Choices are *Enabled*, *Disabled*.

4.3.5.5 Allocate IRQ to PCI VGA

Enable/*Disable* to assign a IRQ for PCI VGA.

Choices are *Yes*, *No*.

4.3.5.6 PCI IDE BusMaster

Set this option to *Enabled* to specify that the IDE controller on the PCI local bus supports bus mastering capability. The settings are *Disabled* or *Enable*d. The default setting is *Disable*d.

4.3.5.7 DMA Channel 0/1/3/5/6/7

Legacy ISA for devices compliant with the original PC AT bus specification, PCI/ISA PnP for devices compliant with the Plug and Play standard whether designed for PCI or ISA bus architecture.

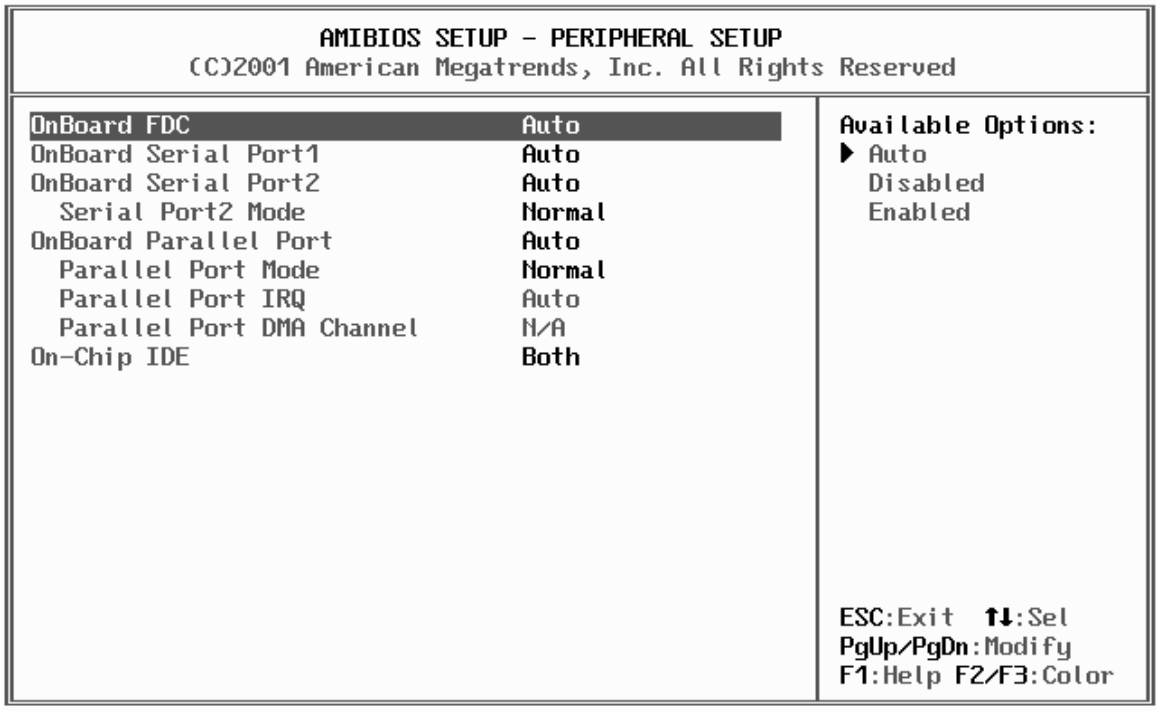
Choices are *ISA/EISA* and *PnP*.

4.3.5.8 IRQ3/4/5/7/9/10/11/14/15

These options specify the bus that the named interrupt request lines (IRQs) are used on. These options allow you to specify IRQs for use by legacy ISA adapter cards. These options determine if AMIBIOS should remove an IRQ from the pool of available IRQs passed to BIOS configurable devices. The available IRQ pool is determined by reading the ESCD NVRAM. If more IRQs must be removed from the pool, the end user can use these PCI/PnP Setup options to remove the IRQ by assigning the option to the *ISA/EISA* setting. Onboard I/O is configurable by AMIBIOS. The IRQs used by onboard I/O are configured as *PCI/PnP.* The settings are *PCI/PnP* or *ISA/EIS*A. The default settings are *PCI/Pn*P.

4.3.6 Peripheral Setup Defaults

This section describes I/O resources assignment for all of on-board peripheral devices.



4.3.6.1 OnBoard FDC

This option enables the floppy drive controller onboard. The settings are *Aut*o, *Enabled,* or *Disable*d.

4.3.6.2 OnBoard Serial Port1

This option enables serial port 1 onboard and specifies the base I/O port address for serial port 1. The settings are *Auto, Disabled, 3F8h, 3E8h, 2E8h,* and *2F8h.* The Fail-Safe default setting is *Aut*o.

4.3.6.3 OnBoard Serial Port2

This option enables serial port 2 onboard and specifies the base I/O port address for serial port 2. The settings are *Aut*o. *Disabled, 3F8h, 2F8h, 3E8h,* and *2E8*h. The default setting is *Aut*o.

4.3.6.4 On Board Parallel Port

There are four optional items *Parallel Port Mode*, *EPP Version*, *Parallel Port IRQ*, and *Parallel Port DMA Channel* used to control on-board parallel port interface while user select I/O base address manually. The following lists are available options of on-board parallel port:

Disabled on-board parallel port function is ineffective and N/A

378h locate IRQ7 for this default I/O address

278h assign this I/O address to LPT1

3BCh assign this I/O address to LPT1

4.3.6.4.1 Parallel Port Mode

This option specifies the parallel port mode. ECP and EPP are both bi-directional data transfer schemes that adhere to the IEEE P1284 specifications. This Parallel Port Mode includes four options “Normal”, “Bi-Dir”, “EPP”, and “ECP”.

Setting	Description
Normal	Uni-direction operation at normal speed
Bi-Dir	Bi-direction operation at normal speed
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bi-directional data transfer driven by the host device.
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits per second ECP provides symmetric bi-directional communicational.

4.3.6.4.2 Parallel Port IRQ

This option is only valid if the **Onboard Parallel Port** option is not set to *Disabled*. This option sets the IRQ used by the parallel port.

4.3.6.4.3 Parallel Port DMA Channel

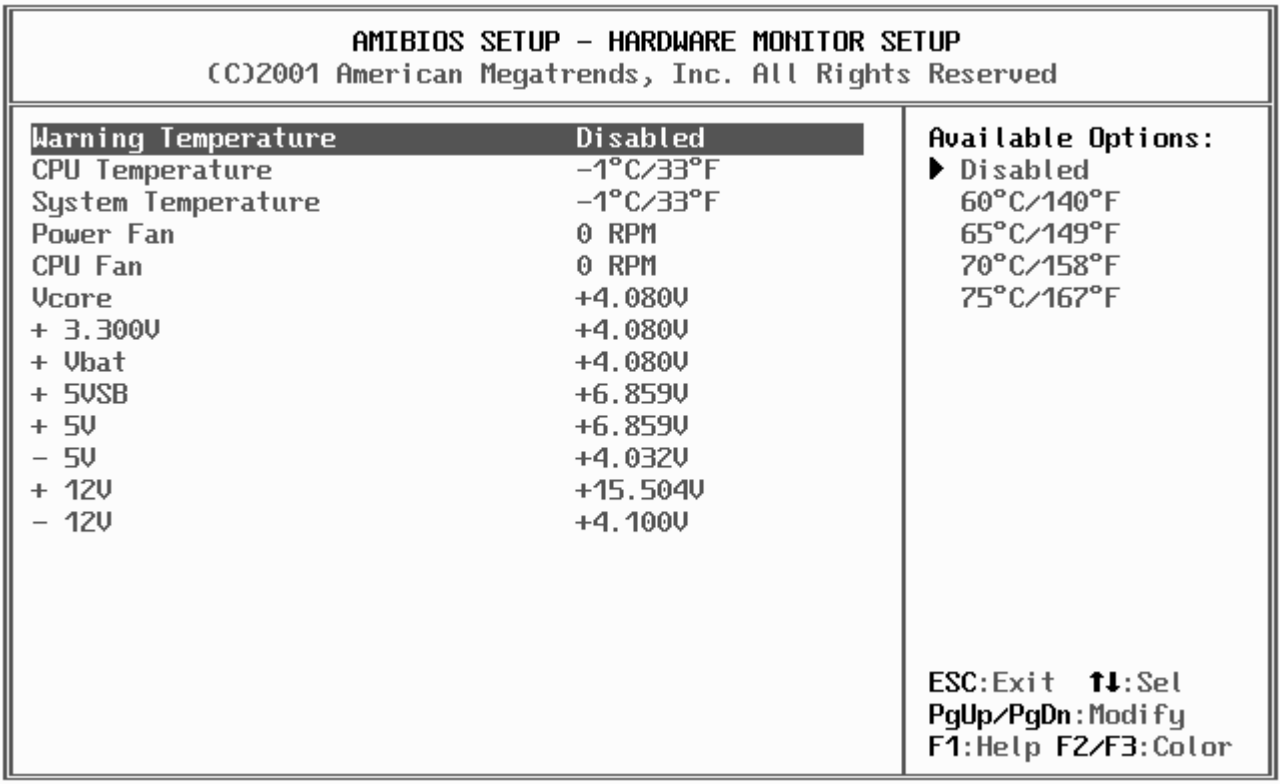
This option is only available if **On Board Parallel Port** is set to fixed I/O address and the setting of **Parallel Port Mode** is ECP. This option sets the DMA channel used by ECP-capable parallel port.

4.3.6.5 On-Chip IDE

This option specifies the onboard IDE controller channels that will be used. The settings are *Primary*, *Secondary*, *Both,* or *Disabled*

4.3.7 Hardware Monitor Setup Defaults

This setup describes current CPU surface temperature status detected from hardware monitor sensor. The status showed on screen will include:



4.3.7.1 Warning Temperature

BIOS Setup Items	Optimal Default	Failsafe Default	Other Options
Warning Temperature	75°C /167°F	75°C /167°F	Disabled, 60°C /140°F, 65°C /149°F, 70°C /158°F, 75°C /167°F,

4.3.7.2 CPU Temperature

4.3.7.3 System Temperature

4.3.7.4 Power Fan

4.3.7.5 System Fan

4.3.7.6 +Vb_{bat}

4.3.7.7 +5VSB

4.3.7.8 +5.000V

4.3.7.9 +12.000V

4.3.7.10 -12.000V

4.3.7.11 -5.000V

4.4 Flash BIOS Utility

Utilize AMI Flash BIOS programming utility to update on-board BIOS for the future new BIOS version. Please contact your technical window to get this utility if necessary.

Note:

Remark or delete any installed Memory Management Utility (such as HIMEM.SYS, EMM386.EXE, QEMM.EXE, …, etc.) in the CONFIG.SYS files before running Flash-programming utility.

5. Driver Installation

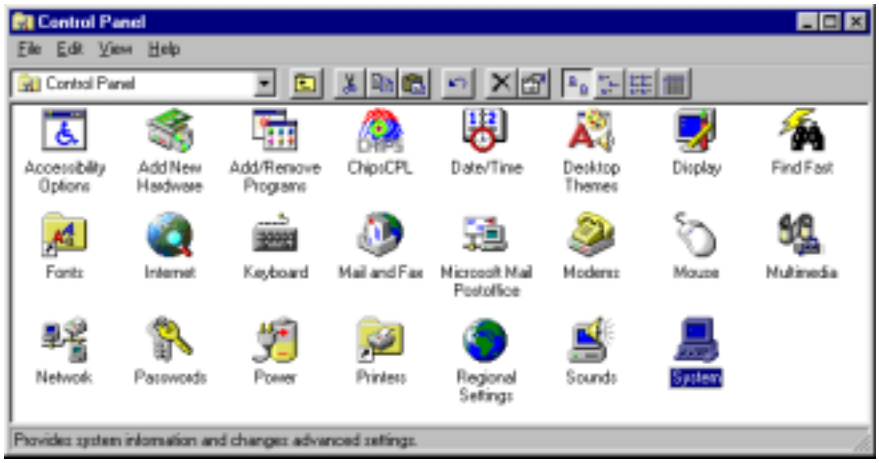
5.1 Driver Installation for Ethernet Adapter

5.1.1 Windows 9x

The best way to install the driver for the Ethernet controller is to use the plug and play system of Windows 9x. The following procedures illustrate how the installation can be done.

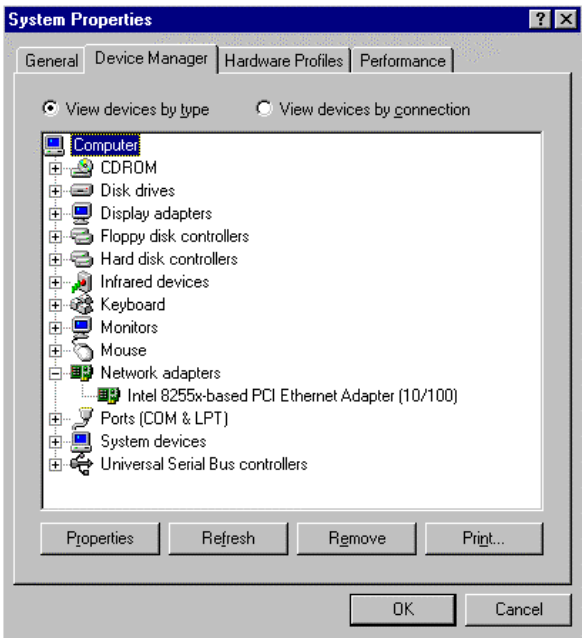
1. If a driver for the Ethernet controller is already installed, it must be removed first. This can be done by following the steps shown below.

    - Click the '*Start*' button, click on '*Settings*' and on '*Control panel*' to open the control panel. Your display should now look as below (possibly with different size and icons):



    - Double click the '*System*' icon (highlighted above).
    - Select the '*Device Manager*' tab.

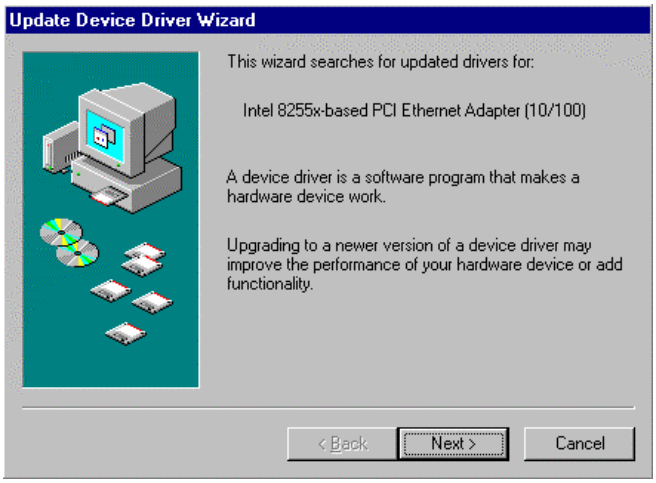
- If the '*Network adapters*' line is present, expand the line and remove the PCI Ethernet Adapter. This is done by selecting the line and clicking the '*Remove*' button. Before removal of the adapter(s), your screen might look like this:



- When all adapters are removed (or none were present), a new driver can be installed now.

2. Reboot the computer.

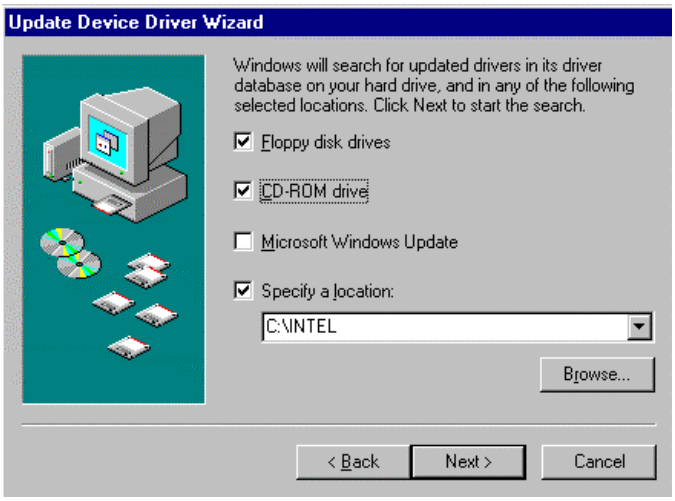
3. During the boot up the network adapter should be detected as shown below. Click the '*Next*' button.


Update Device Driver Wizard
This wizard searches for updated drivers for:
Intel 8255x-based PCI Ethernet Adapter (10/100)
A device driver is a software program that makes a hardware device work.
Upgrading to a newer version of a device driver may improve the performance of your hardware device or add functionality.
< Back
Next >
Cancel

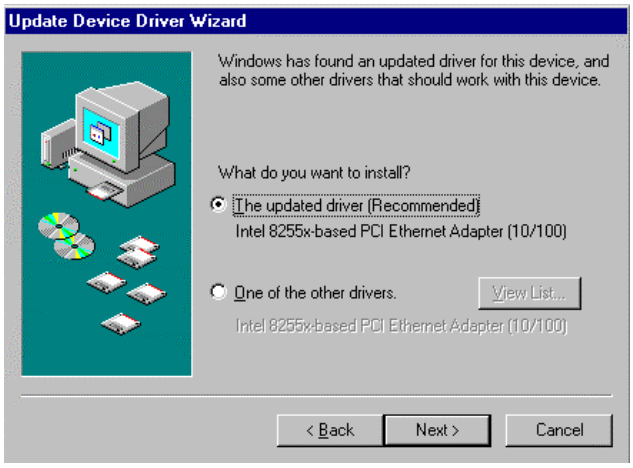
4. Click the '*Next*' button to continue the driver installation.

Update Device Driver Wizard
What do you want Windows to do?
Search for a better driver than the one your device is using now. (Recommended)
Display a list of all the drivers in a specific location, so you can select the driver you want.
< Back
Next >
Cancel

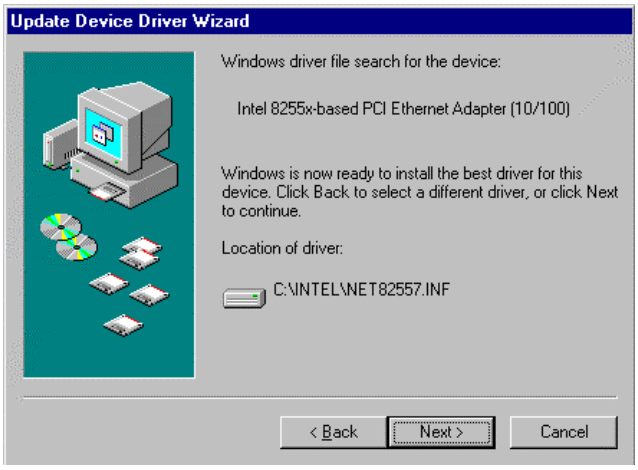
5. Specify the location of network adapter and click '*Next*' (see below).


Update Device Driver Wizard
Windows will search for updated drivers in its driver database on your hard drive, and in any of the following selected locations. Click Next to start the search.
Floppy disk drives
CD-ROM drive
Microsoft Windows Update
Specify a location:
C:\INTEL
Browse...
< Back
Next >
Cancel

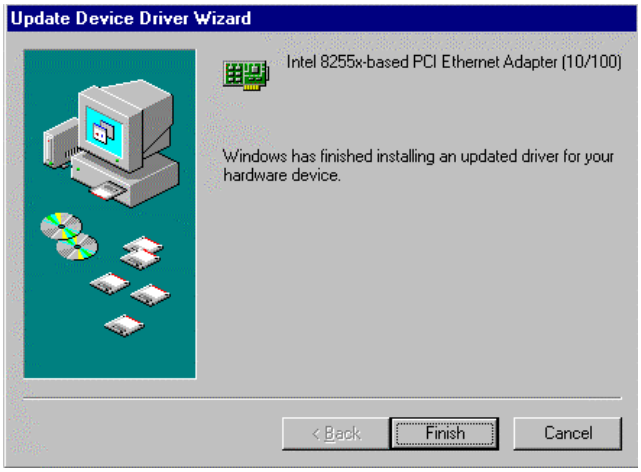
6. Click the '*Next*' button to install the network adapter driver.


Update Device Driver Wizard
Windows has found an updated driver for this device, and also some other drivers that should work with this device.
What do you want to install?
The updated driver (Recommended)
Intel 8255x-based PCI Ethernet Adapter (10/100)
One of the other drivers.
View List...
Intel 8255x-based PCI Ethernet Adapter (10/100)
< Back
Next >
Cancel

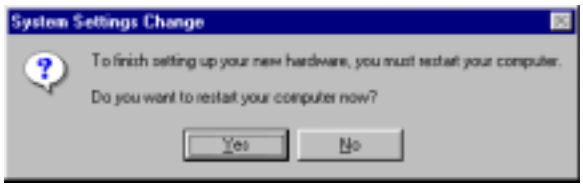
7. Click the '*Next*' button.


Update Device Driver Wizard
Windows driver file search for the device:
Intel 8255x-based PCI Ethernet Adapter (10/100)
Windows is now ready to install the best driver for this device. Click Back to select a different driver, or click Next to continue.
Location of driver:
C:\INTEL\NET82557.INF
< Back
Next >
Cancel

8. Click the '*Finish*' button.


Update Device Driver Wizard
Intel 8255x-based PCI Ethernet Adapter (10/100)
Windows has finished installing an updated driver for your hardware device.
< Back
Finish
Cancel

9. To complete the installation, reboot the computer by clicking the '*Yes*' button in the window shown below.


System Settings Change
To finish setting up your new hardware, you must restart your computer.
Do you want to restart your computer now?
Yes
No

10. After the system restarts, the network adapter should be installed. Protocols, clients etc. may now be installed for the network in use. Further configuration of the adapter may be made in the '*Advanced*' section of the driver properties. These options may be accessed through the '*Network*' icon in the control panel (Select the network adapter, click the '*Properties*' button and select the '*Advanced*' tab).

5.1.2 Windows NT 4.0 Ethernet Installation

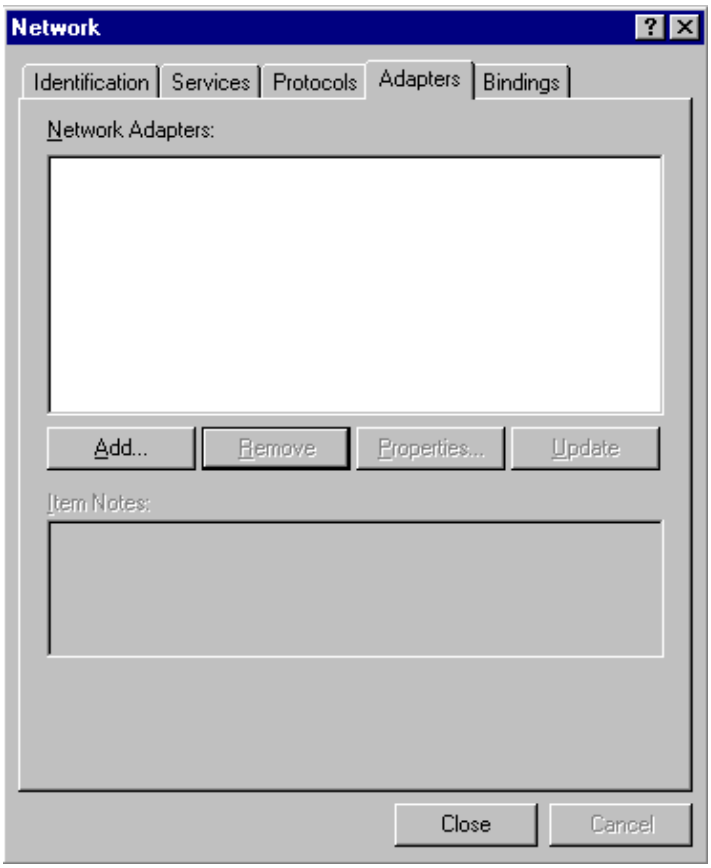
A driver for the Intel 82559 Ethernet controller on board is included in the attached supporting CD-ROM. The driver for this adapter is denoted 'Intel® PRO Adapter'. This driver may be installed in two ways:

- During the installation process where the network may be configured as an integrated part. In this case the adapter may be chosen or auto-detected when the network adapter is to be installed.
- In the network settings after Windows NT 4.0 is installed.

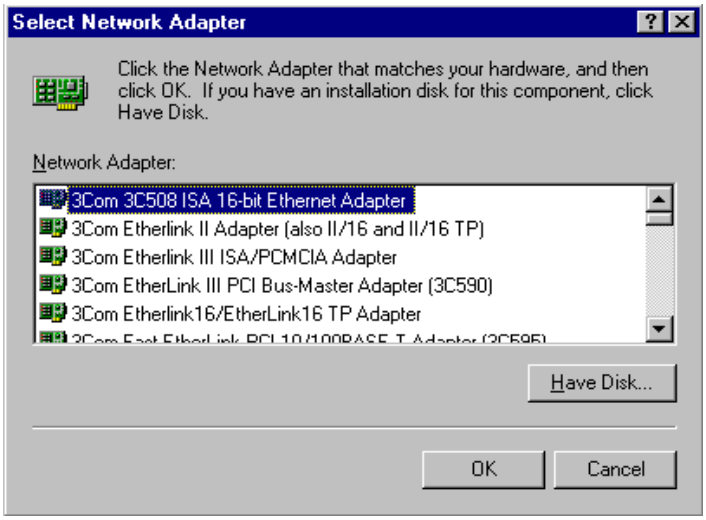
The following procedures describe the steps to install the Network adapter driver on Windows NT 4.0.

1. Click the '*Start*' button on the task bar. Select '*Settings*' and '*Control Panel*' to start the control panel as shown below:

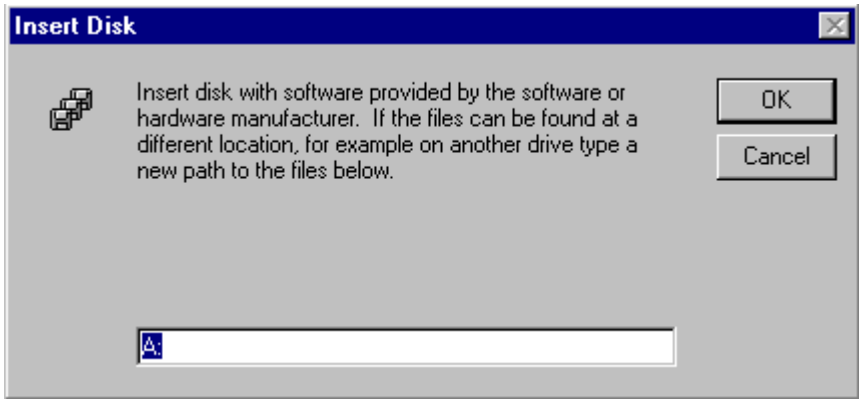
2. Double click the '*Network*' icon and click the '*Adapters*' tab on the following window. A window as the one shown below should now appear.



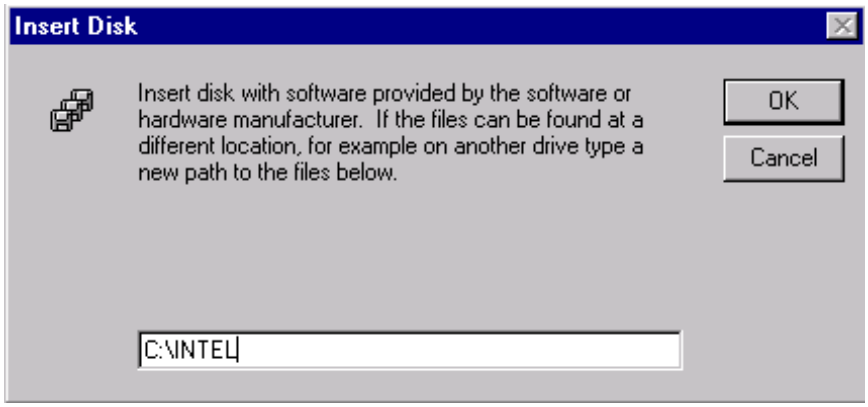
3. Click the '*Add...*' button, and the following window should appear.


Select Network Adapter
Click the Network Adapter that matches your hardware, and then click OK. If you have an installation disk for this component, click Have Disk.
Network Adapter:
3Com 3C508 ISA 16-bit Ethernet Adapter
3Com Etherlink II Adapter (also II/16 and II/16 TP)
3Com Etherlink III ISA/PCMCIA Adapter
3Com EtherLink III PCI Bus-Master Adapter (3C590)
3Com Etherlink16/EtherLink16 TP Adapter
Have Disk...
OK
Cancel

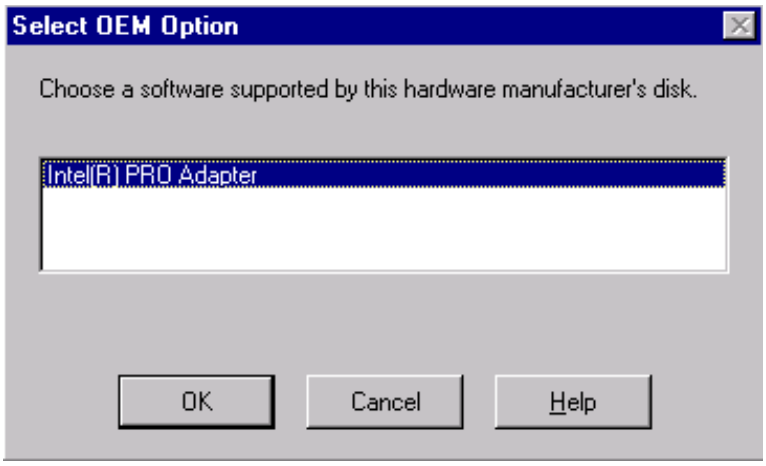
4. Click the '*Have Disk…*' button to install the Network adapter driver from CD-ROM. A window as the one shown below should now appear.


Insert Disk
Insert disk with software provided by the software or hardware manufacturer. If the files can be found at a different location, for example on another drive type a new path to the files below.
OK
Cancel
A:

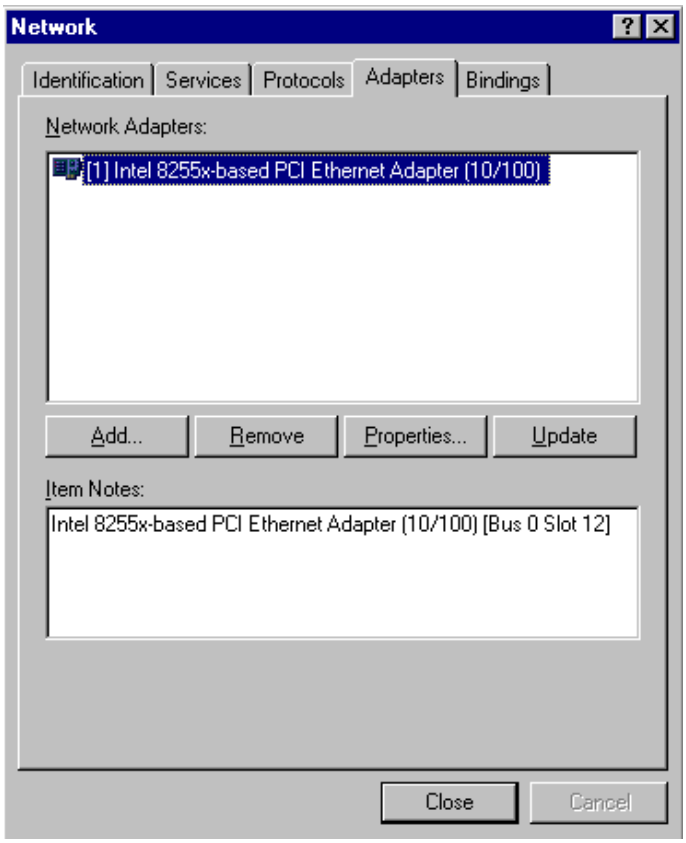
5. Locate the path of Network adapter driver and click the '*OK*' button.


Insert Disk
Insert disk with software provided by the software or hardware manufacturer. If the files can be found at a different location, for example on another drive type a new path to the files below.
OK
Cancel
C:\INTEL

6. Select the '*Intel® PRO Adapter*' from the list (as shown below) and click the '*OK*' button. The Network adapter driver should now be installed.

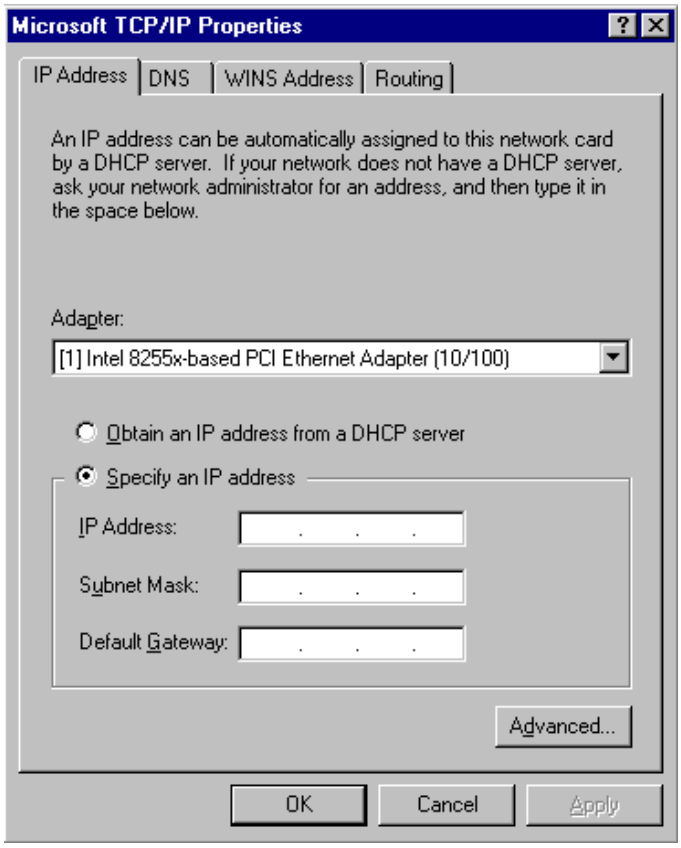


7. After the driver installation is complete, Protocols, Services etc. may now be configured for the network to be used. An example is shown below.

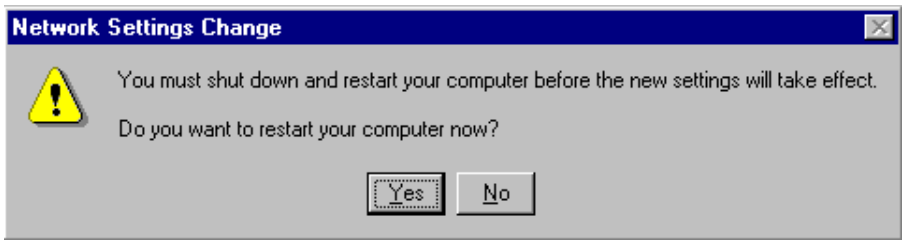


8. Click '*Close*' to accept the settings.

9. IP Address, DNS etc. may now be configured for the network to be used. Click '*OK*' to accept the settings.


Microsoft TCP/IP Properties
IP Address
DNS
WINS Address
Routing
An IP address can be automatically assigned to this network card by a DHCP server. If your network does not have a DHCP server, ask your network administrator for an address, and then type it in the space below.
Adapter:
[1] Intel 8255x-based PCI Ethernet Adapter (10/100)
Obtain an IP address from a DHCP server
Specify an IP address
IP Address:
Subnet Mask:
Default Gateway:
Advanced...
OK
Cancel
Apply

10. To complete the driver installation, reboot the computer by clicking the '*Yes*' button in the window shown below.


Network Settings Change
You must shut down and restart your computer before the new settings will take effect.
Do you want to restart your computer now?
Yes
No

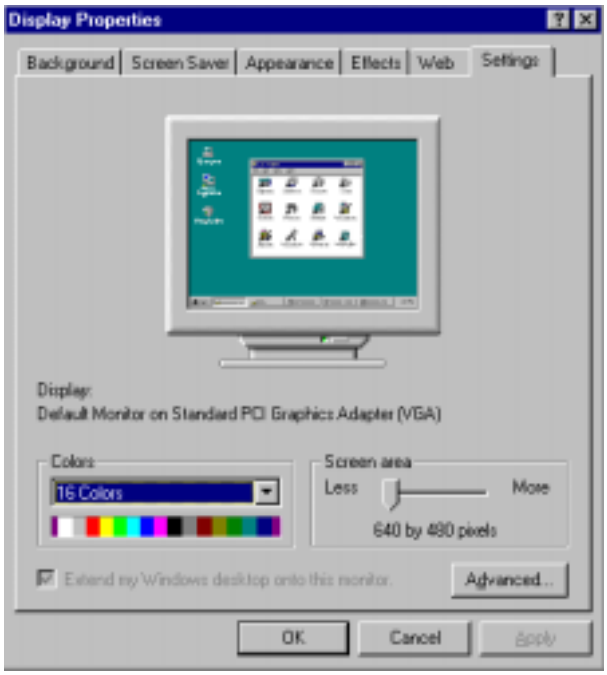
5.2 Driver Installation for Display Adapter

5.2.1 Windows 9x

The following steps will install the display driver for the 'Chips & Technologies 69000 PCI' display controller.

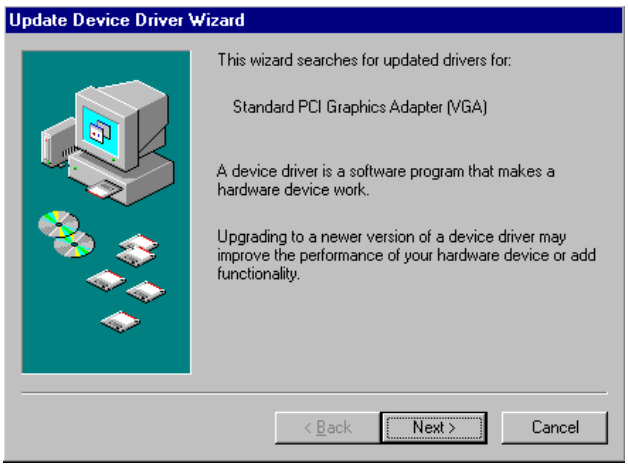
1. Click the '*Start*' button on the task bar, select '*Settings*' and '*Control Panel*' from the sub-menu. This should start the Control Panel as shown below:

2. Double click the '*Display*' icon and select the '*Settings*' tab as shown below.



3. Click the '*Advanced…*' button. This will show the following window. Click the '*Change…*' button in the Adapter Type frame to select another driver. Your display will probably have another driver then the 'Standard PCI Graphics Adapter (VGA)' installed at this moment.

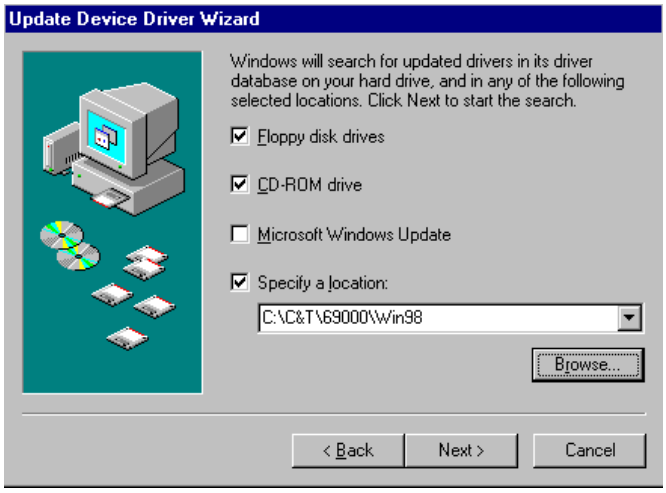
4. Click the '*Next*' to update the display driver.


Update Device Driver Wizard
This wizard searches for updated drivers for:
Standard PCI Graphics Adapter (VGA)
A device driver is a software program that makes a hardware device work.
Upgrading to a newer version of a device driver may improve the performance of your hardware device or add functionality.
< Back
Next >
Cancel

5. Click the '*Next*' to continue the display driver installation.

Update Device Driver Wizard
What do you want Windows to do?
Search for a better driver than the one your device is using now. (Recommended)
Display a list of all the drivers in a specific location, so you can select the driver you want.
< Back
Next >
Cancel

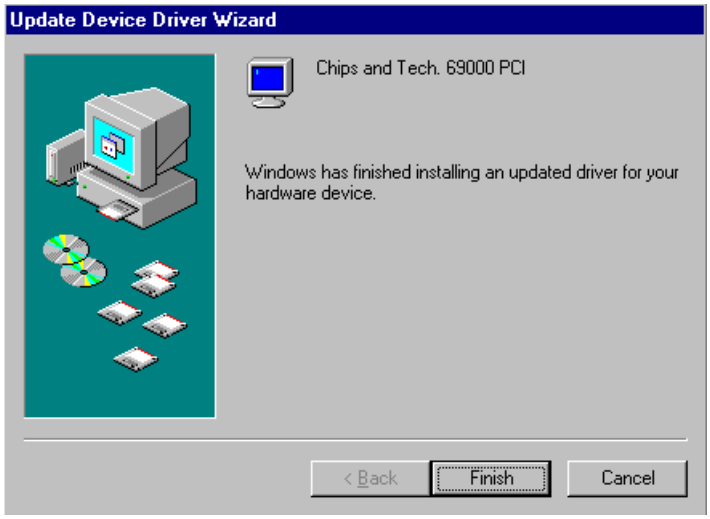
6. Locate the path of Graphics adapter driver and click the '*Next*' button.


Update Device Driver Wizard
Windows will search for updated drivers in its driver database on your hard drive, and in any of the following selected locations. Click Next to start the search.
Floppy disk drives
CD-ROM drive
Microsoft Windows Update
Specify a location:
C:\C&T\69000\Win98
Browse...
< Back
Next >
Cancel

7. The driver files will now be read and the display adapter is shown as the following. Click the '*Next*' button to install the display driver.

Update Device Driver Wizard
Windows driver file search for the device:
Chips and Tech. 69000 PCI
Windows is now ready to install the best driver for this device. Click Back to select a different driver, or click Next to continue.
Location of driver:
C:\CT\69000\WIN98\CHIPS98.INF
< Back
Next >
Cancel

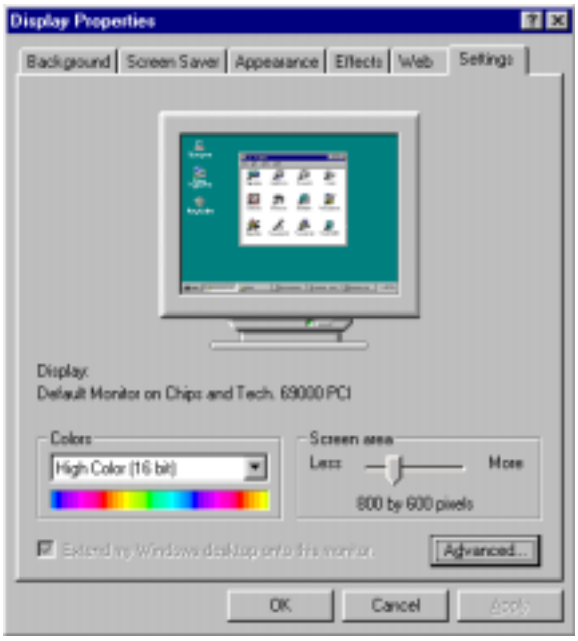
8. Click the '*Finish*' button.


Update Device Driver Wizard
Chips and Tech. 69000 PCI
Windows has finished installing an updated driver for your hardware device.
< Back
Finish
Cancel

9. To complete the display driver installation, reboot the computer by clicking the '*Yes*' button in the window shown below.

System Settings Change
To finish setting up your new hardware, you must restart your computer.
Do you want to restart your computer now?
Yes
No

10. Further configuration of the display adapter may be made from the '*Display Properties*' window (follow step 1 above). The '*Settings*' tab allows you to change resolution, number of colours etc. as shown below.

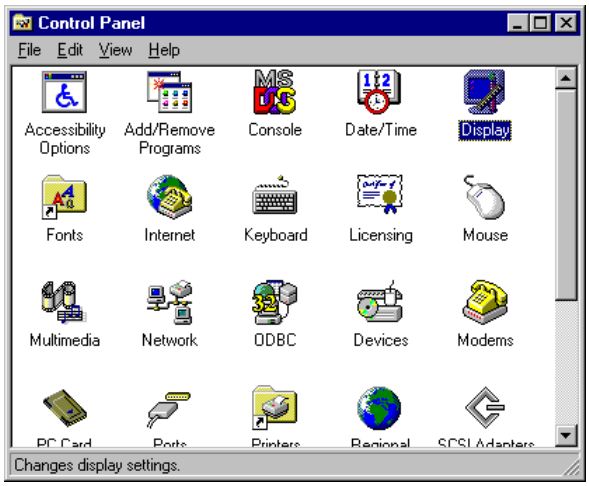


5.2.2 Windows NT 4.0 Display Installation

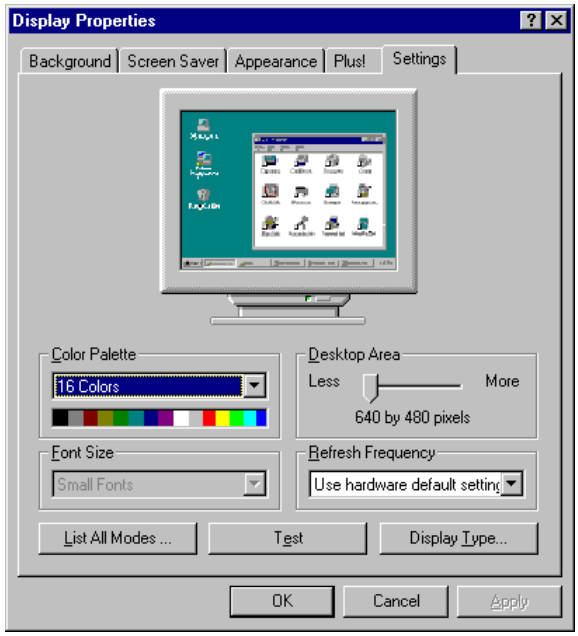
A display driver for Windows NT 4.0 is supplied with the system on the Supporting CD-ROM.

The driver installation may be performed by following steps shown below:

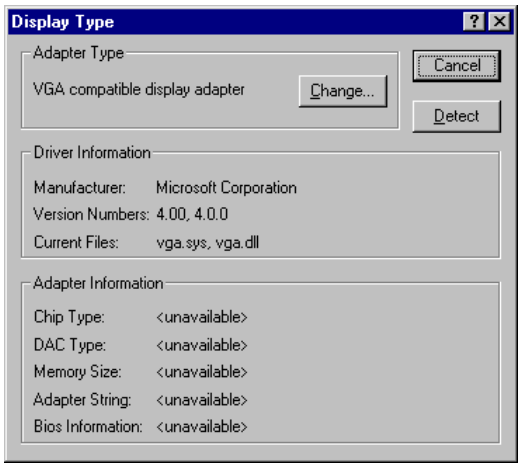
1. Start the control panel by clicking the '*Start*' button, click '*Settings*' and '*Control Panel*' from the sub-menu. Double click the '*Display*' icon in the control panel as shown below.



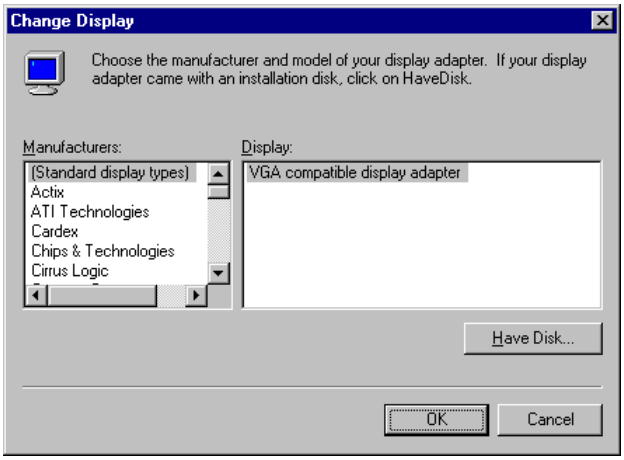
2. On the Display properties window, click the '*Settings*' tab as shown below.



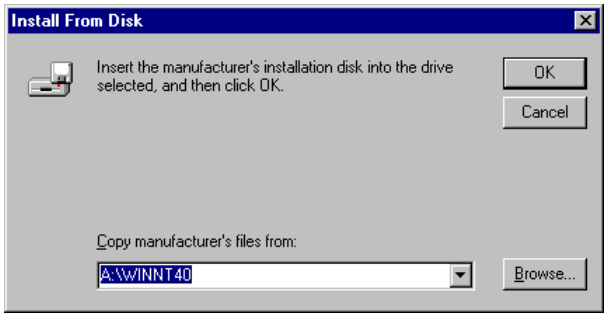
3. Click the '*Display Type…*' button and the following window should appear. Click the '*Change…*' button to select another driver.



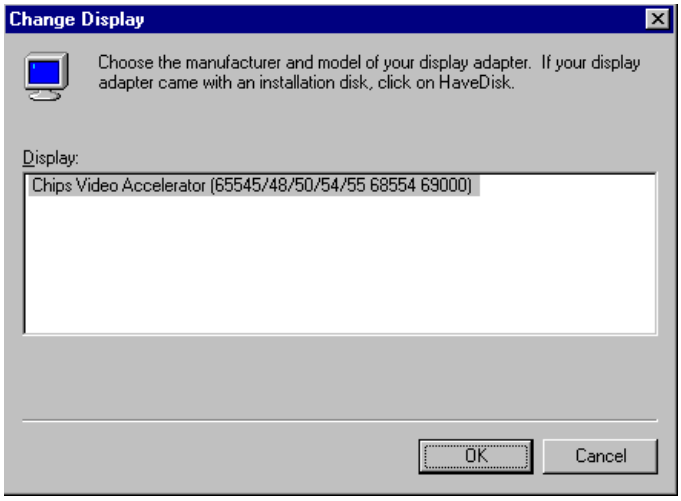
4. Click the '*Have Disk…*' button.



5. The directory for the drivers may now be entered. Type A\:WINNT40 as shown below. Insert the '*Display driver disk*' and click '*OK*'.



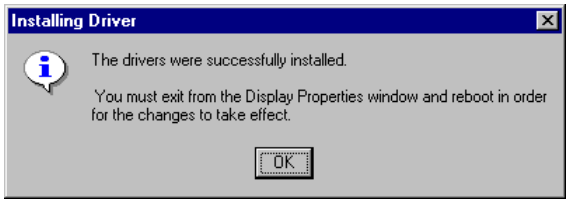
6. The display driver should now be listed as shown below. Click '*OK*' to accept.


Change Display
Choose the manufacturer and model of your display adapter. If your display adapter came with an installation disk, click on HaveDisk.
Display:
Chips Video Accelerator (65545/48/50/54/55 68554 69000)
OK
Cancel

7. Since this driver is not part of the NT4.0 package, the following message will be shown.

Third-party Drivers.
You are about to install a third-party driver.
This driver was written by the hardware vendor, and is only provided here as a convenience. For any problem with this driver, please contact the hardware vendor.
Do you wish to proceed ?
Yes
No

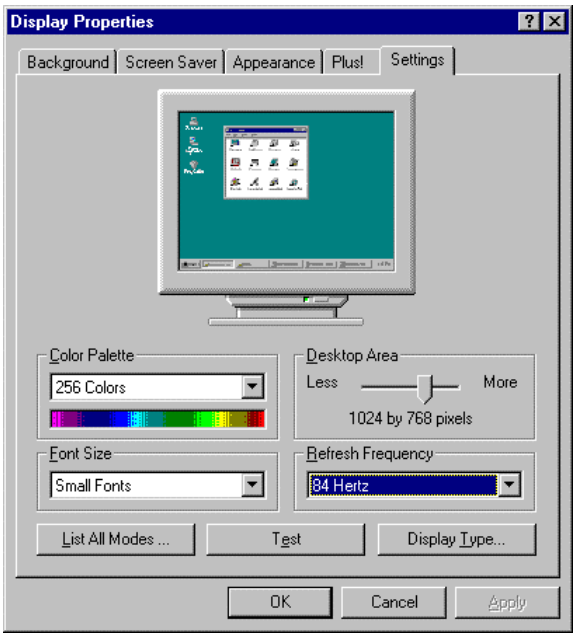
8. To proceed the driver installation, click the '*Yes*' button. The driver will now be installed, and the following message should be shown shortly.


Installing Driver
The drivers were successfully installed.
You must exit from the Display Properties window and reboot in order for the changes to take effect.
OK

9. Click '*OK*' and close the '*Display Type*' and '*Display Properties*' windows by clicking the '*Close*' button in each window.

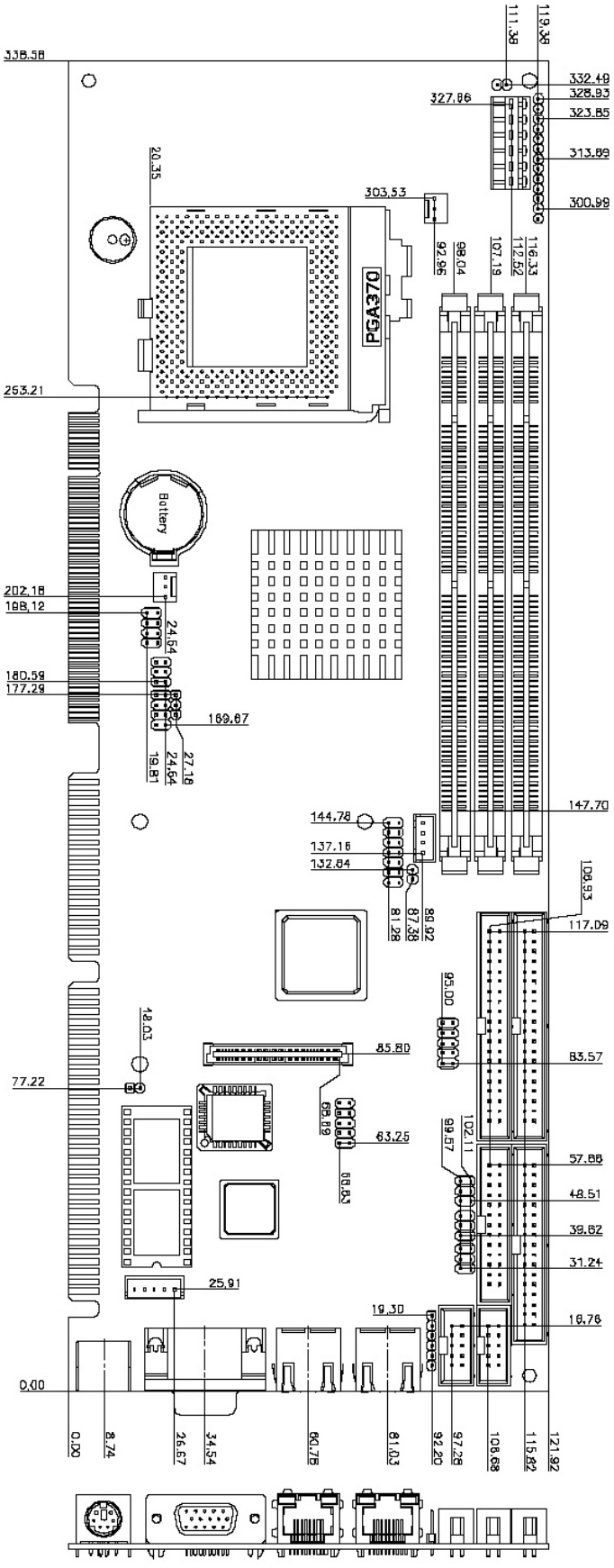
10. After closing the '*Display Properties*' window, the computer must be restarted for the changes to take effect.

11. After the reboot, display resolution etc. may be configured in the '*Display Properties*' window (opened by following steps 1 and 2 above). An example is shown below.



12. Before accepting the new settings by pressing '*OK*', a test should be performed by clicking the '*Test*' button.

6. Measurement Drawing



Appendix A: BIOS Revisions

BIOS Rev.

New Features

Bugs/Problems Solved

Known Problems

Appendix B: System Resources

Memory Map

The following table indicates memory map of ECB-865. The address ranges specify the runtime code length.

Address Range	Description	Note
00000000h-0009FFFFh	System board extension for ACPI BIOS	
000A0000h-000AFFFFh	Intel(R) 82815 Graphics Controller	
000B0000h-000BFFFFh	Intel(R) 82815 Graphics Controller	
000C0000h-000CBFFFh	Intel(R) 82815 Graphics Controller	
000E0000h-000FFFFFh	System board extension for ACPI BIOS	
00100000h-07EFFFFFh	System board extension for ACPI BIOS	
E7900000h-E79FFFFFh	Intel(R) 82801BA PCI Bridge - 244E	
E8000000h-EBFFFFFFh	Intel(R) 82815 Graphics Controller	
EFB00000h-EFDFFFFFh	Intel(R) 82801BA PCI Bridge - 244E	
EFC00000h-EFCFFFFFh	Intel 8255x-based PCI Ethernet Adapter (10/100)	
EFDFF000h-EFDFFFFFh	Intel 8255x-based PCI Ethernet Adapter (10/100)	
EFF80000h-EFFFFFFFh	Intel(R) 82815 Graphics Controller	
FFB80000h-FFBFFFFFh	Intel(r) 82802 Firmware Hub Device	
FFF80000h-FFFFFFFFh	System board extension for ACPI BIOS	
FFFF0000h-FFFFFFFFh	System board extension for PnP BIOS	

I/O – Map

Certain I/O addresses are subject to change during boot as PnP managers may relocate devices or functions. The addresses shown in the table are typical locations.

I/O Port	Description	Note
0000h-000Fh	Direct memory access controller	
0010h-001Fh	Motherboard resources	
0020h-0021h	Programmable interrupt controller	
002Eh-002Fh	Motherboard resources	
0040h-0043h	System timer	
0044h-005Fh	Motherboard resources	
0060h-0060h	Standard 101/102-Key or Microsoft Natural Keyboard	
0061h-0061h	System speaker	
0062h-0063h	Motherboard resources	
0064h-0064h	Standard 101/102-Key or Microsoft Natural Keyboard	
0065h-006Fh	Motherboard resources	
0070h-0071h	System CMOS/real time clock	
0072h-007Fh	Motherboard resources	
0080h-0080h	Motherboard resources	
0081h-0083h	Direct memory access controller	
0084h-0086h	Motherboard resources	
0087h-0087h	Direct memory access controller	
0088h-0088h	Motherboard resources	
0089h-008Bh	Direct memory access controller	
008Ch-008Eh	Motherboard resources	
008Fh-008Fh	Direct memory access controller	
0094h-009Fh	Motherboard resources	
00A0h-00A1h	Programmable interrupt controller	
00A2h-00BFh	Motherboard resources	
00C0h-00DFh	Direct memory access controller	
00C0h-00DEh	Direct memory access controller	
00E0h-00EFh	Motherboard resources	
00F0h-00FFh	Numeric data processor	
0170h-0177h	Secondary Ultra ATA Controller	
0170h-0177h	Intel(R) 82801BA Ultra ATA Storage Controller - 244B	
01F0h-01F7h	Primary Ultra ATA Controller	
01F0h-01F7h	Intel(R) 82801BA Ultra ATA Storage Controller - 244B	
02F8h-02FFh	Communications Port (COM2)	
0376h-0376h	Secondary Ultra ATA Controller	
0376h-0376h	Intel(R) 82801BA Ultra ATA Storage Controller - 244B	
0378h-037Fh	Printer Port (LPT1)	
03B0h-03BBh	Intel(R) 82815 Graphics Controller	

I/O Port	Description	Note
03C0h-03DFh	Intel(R) 82815 Graphics Controller	
03F0h-03F3h	Standard Floppy Disk Controller	
03F4h-03F5h	Standard Floppy Disk Controller	
03F6h-03F6h	Primary Ultra ATA Controller	
03F8h-03FFh	Communications Port (COM1)	
0400h-047Fh	Motherboard resources	
0440h-044Fh	Motherboard resources	
04D0h-04D1h	Motherboard resources	
0CF8h-0CFFh	PCI bus	
C000h-CFFFh	Intel(R) 82801BA PCI Bridge - 244E	
CE80h-CEBFh	Intel(R) PRO/100 VE Network Connection	
CF00h-CF3Fh	Intel 8255x-based PCI Ethernet Adapter (10/100)	
DE80h-DE9Fh	Intel(R) 82801BA/BAM USB Universal Host Controller - 2442	
DF00h-DF1Fh	Intel(R) 82801BA/BAM USB Universal Host Controller - 2444	
FF00h-FF07h	Primary Ultra ATA Controller	
FF00h-FF0Fh	Intel(R) 82801BA Ultra ATA Storage Controller - 244B	
FF08h-FF0Fh	Secondary Ultra ATA Controller	

Interrupt Usage.

The onboard Intel 82801BA provides an ISA compatible interrupt controller with functionality as two 8259A interrupt controllers. The two controllers are cascaded to provide 13 external interrupts.

The actual interrupt settings depend on the PnP handler, the table below indicates the typical settings.

Interrupt	Description	Note
IRQ0	System timer	
IRQ1	Standard 101/102-Key or Microsoft Natural Keyboard	
IRQ2	Programmable interrupt controller	
IRQ3	Communications Port (COM2)	
IRQ4	Communications Port (COM1)	
IRQ5	ACPI IRQ Holder for PCI IRQ Steering	
IRQ5	Intel(R) 82801BA/BAM USB Universal Host Controller - 2442	
IRQ5	Intel 8255x-based PCI Ethernet Adapter (10/100)	
IRQ6	Standard Floppy Disk Controller	
IRQ7	Printer Port (LPT1)	
IRQ8	System CMOS/real time clock	
IRQ9	SCI IRQ used by ACPI bus	
IRQ10	Intel(R) PRO/100 VE Network Connection	
IRQ10	ACPI IRQ Holder for PCI IRQ Steering	
IRQ10	Intel(R) 82801BA/BAM USB Universal Host Controller - 2444	
IRQ10	ACPI IRQ Holder for PCI IRQ Steering	
IRQ11	Intel(R) 82815 Graphics Controller	
IRQ11	ACPI IRQ Holder for PCI IRQ Steering	
IRQ12	PS/2 Compatible Mouse Port	
IRQ13	Numeric data processor	
IRQ14	Intel(R) 82801BA Ultra ATA Storage Controller - 244B	
IRQ14	Primary Ultra ATA Controller	
IRQ15	Intel(R) 82801BA Ultra ATA Storage Controller - 244B	
IRQ15	Secondary Ultra ATA Controller	

DMA-channel Usage

The DMA circuitry incorporates the functionality of two 8237 DMA controllers with seven programmable channels. The controllers are referenced DMA Controller 1 for channels 0-3 and DMA Controller 2 for channels 4-7. Channel 4 is by default used to cascade the two controllers.

DMA-channel	Description	Note
DMA0	Available for PC/104 interface & PCI slot	
DMA1	Available for PC/104 interface & PCI slot	
DMA2	Standard Floppy Disk Controller	
DMA3	Parallel port, if using ECP mode	
DMA4	Used for cascading	
DMA5	Available for PC/104 interface & PCI slot	
DMA6	Available for PC/104 interface & PCI slot	
DMA7	Available for PC/104 interface & PCI slot	

Appendix C: AMIBIOS Power-On Self Test

Every time the system is powered on, AMIBIOS executes a power-on self test. In case of errors they are reported in one of two ways. If the error occurs before the display device is initialised, a series of beeps sound. Beep codes indicate that a fatal error has occurred. AMIBIOS Beep Codes are described in the table below.

If it beeps…	Then…
1, 2, or 3 times	Re-insert the memory SIMMs. If the system still beeps replace the memory.
6 times	Try a different keyboard or replace the keyboard fuse if the keyboard has one.
8 times	There is an error on the Video adapter or the Video RAM
9 times	The BIOS ROM chip is bad. The system probably needs a new BIOS ROM chip.
11 times	Re-insert the cache memory on the board. If it still beeps, replace the cache memory.
4, 5, 7, or 10 times	Fatal error.

If the error occurs after the display device is initialised, an error message is displayed.

APPENDIX D: AMIBIOS POST Check Point List

AMIBIOS provides all IBM standard Power On Self Test (POST) routines as well as enhanced AMIBIOS POST routines. The POST routines support CPU internal diagnostics. The POST checkpoint codes are accessible via the Manufacturing Test Port (I/O port 80h).

Whenever a recoverable error occurs during the POST, the system BIOS will display an error message describing the message and explaining the problem in detail so that the problem can be corrected.

During the POST, the BIOS signals a checkpoint by issuing one code to I/O address 80H. This code can be used to establish how far the BIOS has executed through the power-on sequence and what test is currently being performed. This is done to help troubleshoot faulty system board.

If the BIOS detects a terminal error condition, it will halt the POST process and attempt to display the checkpoint code written to port 80H. If the system hangs before the BIOS detects the terminal error, the value at port 80H will be the last test performed. In this case, the terminal error cannot be displayed on the screen. The following POST checkpoint codes are valid for all AMIBIOS products with a core BIOS date of 07/15/95 version 6.27 (Enhanced).

Uncompressed Initialization Codes — The uncompressed initialization checkpoint hex codes are listed in order of execution:

Code	Description
D0	NMI is disabled. CPU ID saved. INIT code checksum verification will be started.
D1	Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh, and going to 4GB flat mode.
D3	To start memory sizing.
D4	Returning to real mode. Executing any OEM patches and setting the stack next.
D5	Passing control to the uncompressed code in shadow RAM at E000:0000h. The INIT code is copied to segment 0 and control will be transferred to segment 0.
D6	Control is in segment 0. Next, checking if <Ctrl><Home> was pressed and verifying the system BIOS checksum. If either <Ctrl><Home> was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.
D7	To pass control to interface module.
D8	Main BIOS runtime code is to be decompressed.
D9	Passing control to the main system BIOS in shadow RAM next.

Bootblock Recovery Codes — The bootblock recovery checkpoint hex codes are listed in order of execution:

Code	Description
E0	The onboard floppy controller if available is initialized. Next, beginning the base 512KB memory test.
E1	Initializing the interrupt vector table next.
E2	Initializing the DMA and Interrupt controllers next.
E6	Enabling the floppy drive controller and Timer IRQs. Enabling internal cache memory.
ED	Initializing the floppy drive.
EE	Start looking for a diskette in drive A: and read first sector of the diskette.
EF	A read error occurred while reading the floppy drive in drive A: .
F0	Next, searching for the AMIBOOT.ROM file in the root directory.
F1	The AMIBOOT.ROM file is not in the root directory.
F2	Next, reading and analyzing the floppy diskette FAT to find the clusters occupied by the AMIBOOT.ROM file.
F3	Start reading AMIBOOT.ROM file, cluster by cluster.
F4	The AMIBOOT.ROM file is not the correct size.
F5	Next, disabling internal cache memory.
FB	Next, detecting the type of Flash ROM.
FC	Erasing the Flash ROM.
FD	Programming the Flash ROM
FF	Flash ROM programming was successful. Next, restarting the system BIOS.

Uncompressed Initialization Codes — The following runtime checkpoint hex codes are listed in order of execution. These codes are uncompressed in F0000h shadow RAM.

Code	Description
03	The NMI is disabled. Next, checking for a soft reset or a power on condition.
05	The BIOS stack has been built. Next, disabling cache memory.
06	Uncompressing the POST code next.
07	Next, initializing the CPU and the CPU data area.
08	The CMOS checksum calculation is done next.
0B	Next, performing any required initialization before the keyboard BAT command is issued.
0C	The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller.
0E	The keyboard controller BAT command result has been verified. Next, performing any necessary INIT after the K/B controller BAT command test.
0F	The keyboard command byte is written next.
10	Next, issuing the pin 23 and 24 blocking and unblocking commands.
11	Next, checking if the <End> or <Ins> keys were pressed during power on.
12	To initialize CMOS if the *initialize CMOS RAM in every boot* is set or the <End> key is pressed. Going to disable DMA and Interrupt controllers.
13	The video display has been disabled. Port B has been initialized. Next, initialising the chipset.
14	The 8254 timer test will begin next.
19	The 8254 timer test is over. Starting the memory refresh test next.
1A	The memory refresh line is toggling. Checking the 15us on/off time next.
23	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24	The configuration or setup required before interrupt vector initialization has completed. Interrupt vector init. is about to begin
25	Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.

Code	Description
2A	Bus initialization system, static, output devices will be done next, if present.
2B	Passing control to the video ROM to perform any required configuration before the video ROM test.
2C	To look for optional video ROM and give control.
2D	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control.
2E	Completed podt-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. Look for retrace checking next.
31	Display memory R/W test or retrace checking failed. To do alternate display retrace checking.
32	Alternate display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking is over. Setting the display mode next.
37	The display mode is set. Displaying the power on message next.
38	Initializing the bus input, IPL, and general devices next, if present.
39	Displaying bus initialization error message.
3A	The new cursor position has been read and saved. Displaying the *Hit <DEL>* message next.
40	Preparing the descriptor tables next.
42	Entering protected mode for the memory test next.
43	Entered protected mode. Enabling interrupts for diagnostics mode next.
44	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45	Data initialized. Checking for memory wraparound at 0:0 and finding the total System memory size next.
46	The memory wraparound test has completed. The memory size calculation has been done. Writing patterns to test memory next.
47	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory test.
48	Patterns written in base memory. Determining the amount of memory below 1MB next.
49	The amount of memory below 1MB has been found and verified. Determining the amount of memory above 1MB memory next.

Code	Description
4B	The amount of memory above 1MB has been found and verified. Checking for a soft reset and clearing the memory below 1MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.
4C	The memory below 1MB has been cleared via a soft reset. Clearing the memory above 1MB next.
4D	The memory above 1MB has been cleared via soft reset. Saving the memory size next. Going to checkpoint 52h next.
4E	The memory test started, but not as the result of a soft reset. Displaying the first 64KB memory size next.
4F	Memory size display started. This will be updated during memory test. Performing the sequential and random memory test next.
50	Memory testing/initialization below 1MB completed. Going to adjust displayed memory size for relocation and shadowing.
51	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1MB next.
52	The memory above 1MB has been tested and initialized. Saving the memory size information next.
53	The memory size information and the CPU registers are saved. Entering real mode next.
54	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57	The A20 address line, parity, and the NMI are disabled. Adjusting the memory sizedepending on relocation and shadowing next.
58	The memory size was adjusted for relocation and shadowing. Clearing the *Hit <DEL>* message next.
59	The *Hit <DEL>* message is cleared. The *<WAIT…>* message is displayed. Staring the DMA and interrupt controller test next.
60	The DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.

Code	Description
81	A keyboard reset error or stuck key was found. Issuing the keyboard Controller interface test command next.
82	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83	Command byte written, Global data init done. To check for lock-key.
84	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85	The memory size check is done. Displaying a soft error and checking for a password or bypassing Setup next.
86	Password checked. About to do programming before setup.
87	The programming before Setup has completed. Uncompressing the Setup code and executing the AMIBIOS Setup utility next.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	The programming after Setup has completed. Displaying the power on Screen message next.
8B	The first screen message has been displayed. The <WAIT…> message is displayed. Performing the PS/2 mouse check and extended BIOS data area allocation check next.
8C	Programming the Setup options next.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	The floppy drive controller has been configured. Configuring the hard disk drive controller next.
95	Initializing the bus option ROMs from C800 next.
96	Initializing before passing control to the adaptor ROM at C800.
97	Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next.
98	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
99	Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next.

Code	Description
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after setting the RS-232 base address. Performing any required Initialization before the Coprocessor test next.
9C	Required initialization before the Coprocessor test is over. Initializing the Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after the Coprocessor test is complete. Checking the extended Keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.
A2	Displaying any soft errors next.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7	NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.
A8	Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next.
A9	Returned from adaptor ROM at E000h control. Performing any initialisation required after the E000 option ROM had control next.
AA	Initialization after E000 option ROM control has completed. Displaying the system configuration next.
AB	Building the multiprocessor table, if necessary.
AC	Uncompressing the DMI data and initializing DMI POST next.
B0	The system configuration is displayed.
B1	Copying any code to specific areas.
00	Code copying to specific areas is done. Passing control to INT 19 h boot loader next.